Assembly Solutions for Cost-Effective Heterogeneous Integration with Disparate Die Types

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Abstract

The semiconductor industry is driving to enable high volume integration of disparate die types via Heterogeneous Integration. These die can come from a range of wafer sizes fabricated in different technology nodes. This emerging package type creates new challenges regarding assembly efficiency and yield. Traditionally, flip-chip assembly process flows have utilized a single placement tool for the placement of the single die type onto the target substrate. For applications with multiple die types, a series of placement tools have been configured in a production line, with each tool dedicated to the placement of a specific die type. This paper and presentation explore the implications of this type of solution in the era of Heterogeneous Integration. Impacts on product yield, throughput, manufacturing efficiency, and overall cost of assembly will be explored for a broad range of Heterogeneous Integration die configurations. Based on a sensitivity analysis for the range of die types expected in these applications, a novel approach to optimization of overall assembly economics will be proposed. The appropriateness of this novel approach will be explored for a range of packaging solutions, including Flip-Chip, 2.5D, 3D, and Fan-Out.

Keywords

Advanced Packaging, Heterogeneous Integration, 2.5D Assembly, Fan-Out.

I. Introduction

While transistor scaling continues, the economic improvements derived from this scaling, typically referred to as "Moore's Law," have been diminishing. For example, over the past decade, at nodes below 22nm, the associated costs to design and introduce new products have increased by a factor of 7.75. (Figure 1, Reference #1).

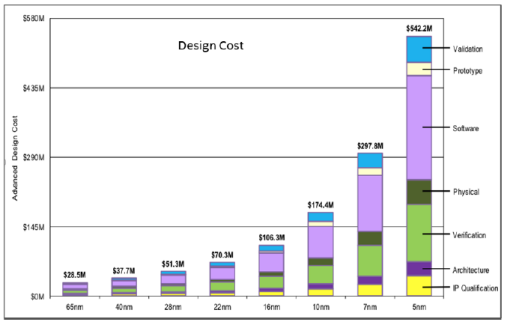

Figure 1: Design cost by node

The prevailing packaging solution to address this challenge is called Heterogeneous Integration (HI). Many studies have focused on a chip to chip signaling, power distribution, materials, thermals, bonding metallurgy, and design methodologies. Interface open standards such as UCI Express (Reference #2) attempt to establish a common specification for HI implementation.

An assessment of the economic implications for various placement tool process flows has not been conducted.

Placement tool costs can be subdivided into five major categories: yield, equipment depreciation, operators, floor space, and equipment utilization.

The "pick and place" assembly of multiple disparate die in a heterogeneous integration package traditionally uses multiple placement tools. Each unique tool is dedicated for placement of a specific die type and/or wafer type.

A novel approach is to execute the complete placement of all die types for a given Heterogeneous Integrated package within a single tool.

A sensitivity analysis for a broad range of die configurations can be assessed by modeling the impact on the five major cost categories for the scenario of multiple dedicated placement tools vs a single tool solution.

II. HI Circuit Characteristics

A. Device types and quantity per substrate

The number of devices per HI circuit ranges from a minimum of two device types and may be as high as 8 unique devices. These die typically range in size from .5 x .5 mm up to 20 x 20 mm. The quantity of each die per substrate can range from one to as many as 8.

Each die has a specific function, ranging from processor to memory, to sensing, to data transmission. A typical configuration with four die types, and a maximum of 8 die for one die type is shown in Figure 2.

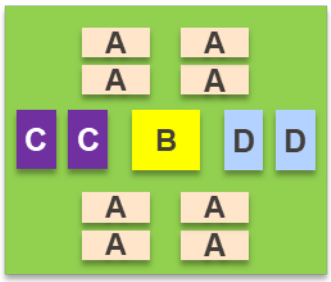

Figure 2: Typical HI device configuration

B. Substrate size and quantity

Substrates upon which devices are mounted can range from traditional singulated HDI organic to singulated silicon interposers to a substrate-less Wafer or Panel fan-out. In the case of singulated organic substrates, these are typically presented to the "pick and place" assembly tool via a JEDEC standard tray (or Gen2 JEDEC tray in the future). At substrate dimensions up to 31 x 44mm, up to 28 circuit substrates can be loaded in one JEDEC tray (Figure 3). Future Gen2 JEDEC trays can hold up to 56 of this sized circuit substrates.

A substrate-less Wafer level fan-out carrier offers an assembly area for approximately 38 of this sized circuit, while a JEDEC standard panel fan-out carrier, which has a 600mm x 600mm assembly area, supports up to 247 of this sized circuit.

The number of circuits per carrier significantly impacts the throughput of a single cell placement solution, as wafer exchange time is amortized over a much larger number of placements for a specific die type. (Table 1)

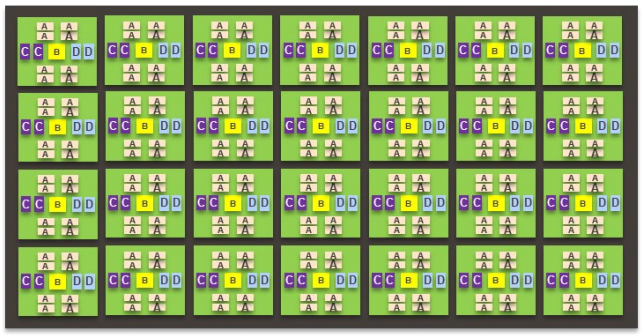

Figure 3: JEDEC Tray with 28 Substrates

Carrier Type	Circuits per Carrier
JEDEC Tray	28
Wafer Level Fan-Out Carrier	38
Gen2 JEDEC Tray (future)	56
Semi-Standard Panel	247

Table 1: 31mm x 44mm circuit capacity by carrier type

III. Pick and Place Tool Characteristics

Traditional die pick & place line solutions have been optimized based on the premise that a single die will be placed on a single substrate. This is the typical flip-chip application, which is the dominant "advanced packaging" application in the market today.

In the case of Heterogeneous Integrated devices, the solution has been to configure multiple systems in series with each other. Each system is tooled and dedicated to a specific wafer type and die type.

There are several challenges with this approach. The first challenge is that the line is unbalanced, as some systems may be placing 8 or more devices, while some could be placing only one die (or even zero devices if there are more systems than die types to be placed). This results in an overall "effective throughput" per system that is as low as 13% of a single system solution. Constant re-arranging of the line would be required to optimize the assembly flow for different HI circuit configurations, which is impractical in a production environment. (Figure 4)

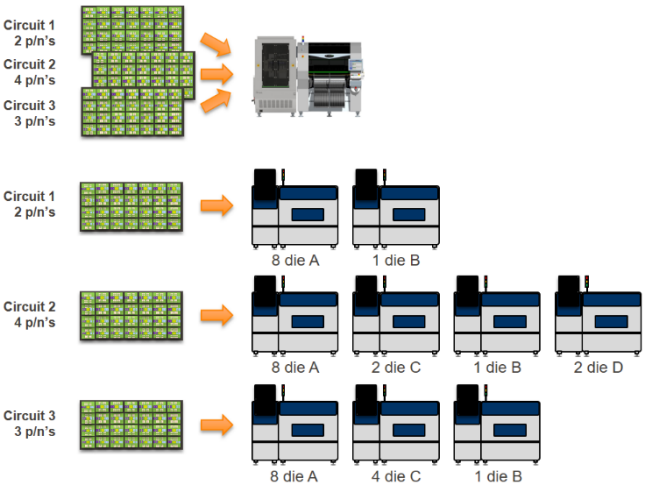

Figure 4: Single System vs. Multiple dedicated System Line

The second challenge is that the constant flattening and then flexing of the substrate can cause die float, as can movement out of and into multiple systems, impacting placement accuracy. Finally, moving substrates between 8 dedicated systems in a line increases placement, fiducial find, and potentially temperature variability, which further degrade placement accuracy. Based on typical system variability data, it is estimated that all these factors will increase the defective placement ppm per device from a typical value of 100ppm to 400ppm for a 4-die HI device.

The third challenge is that increased operator attention will be required per line with up to 8 machines in a line, as will increased floor space. This will increase the overall OPEX cost for the line proportional to the number of systems in the line.

The fourth challenge is utilization. Creating dedicated lines per circuit configuration versus a single cell that can handle any circuit will reduce typical utilization. In addition, material scheduling and downtime typically reduce a Single system solution to 85% utilization. With a 4-system solution, these "multi-system" factors are expected to reduce utilization further to, at best, 60%.

III. Throughput Sensitivity Analysis

To better understand the overall impact of these various parameters on Heterogeneous Integration assembly economics, a mathematical model was created to allow for a comprehensive sensitivity analysis.

As mentioned, the most critical factors are the time it takes to automatically change wafers and change associated end effector tooling to support a new die type, the number of circuits to be assembled per carrier, and the number of unique die types to be assembled per circuit.

A. Impact of Circuits per Carrier and Wafer & Tooling Change Time

Table 2 summarizes the relative throughput of assembled circuits for a Single System per Circuit solution vs. a Single Die per System solution. The comparison is made both for a Single System solution configured with a single wafer table as well as a Single System solution configured with dual wafer tables. The time to exchange unique wafers and end effector tooling for unique die types was varied from 15 seconds to 60 seconds. For this example, it was assumed the circuit had four unique die types, with quantity of die per die type of 8,4,2,1 respectively.

From Table 2, it can be seen that over the full range of scenarios for circuits per carrier and wafer + tooling exchange time, that a Single System per Circuit solution delivers superior throughput. This advantage ranges from 12% in the corner case of only 4 circuits per carrier and 60 second wafer + tooling exchange time on a Single Wafer Table system, up to 93% advantage when there are 1,024 circuits on a carrier and an exchange time of only 15 seconds.

	Wafer Exchange Time, Single Wafer Table System (sec)									
Circuits per Carrier	15	20	25	30	35	40	45	50	55	60
4	31%	37%	43%	49%	56%	61%	68%	74%	81%	88%
8	22%	25%	28%	31%	35%	38%	41%	44%	47%	51%
16	17%	19%	21%	22%	24%	25%	27%	29%	30%	32%
32	15%	16%	17%	17%	18%	19%	20%	21%	22%	22%
64	14%	15%	15%	15%	15%	16%	16%	17%	17%	17%
128	14%	14%	14%	14%	14%	15%	15%	15%	15%	15%
256	14%	14%	14%	14%	14%	14%	14%	14%	14%	14%
512	13%	13%	14%	14%	14%	14%	14%	14%	14%	14%
1024	13%	13%	13%	13%	13%	13%	13%	14%	14%	14%

Relative Throughput per Circuit: Single System Solution compared to System per Die Type Solution

	Wafer Exchange Time, Dual Wafer Table System (sec)									
Circuits per Carrier	15	20	25	30	35	40	45	50	55	60
4	16%	19%	22%	25%	28%	31%	34%	37%	41%	43%
8	11%	13%	15%	16%	18%	19%	21%	22%	24%	26%
16	9%	10%	11%	11%	12%	13%	14%	15%	16%	16%
32	8%	8%	9%	9%	10%	10%	10%	11%	11%	12%
64	8%	8%	8%	8%	8%	8%	9%	9%	9%	9%
128	8%	8%	8%	8%	8%	8%	8%	8%	8%	8%
256	7%	8%	8%	8%	8%	8%	8%	8%	8%	8%
512	7%	7%	7%	7%	7%	7%	8%	8%	8%	8%
1024	7%	7%	7%	7%	7%	7%	7%	7%	7%	7%

Relative throughput per Circuit: Single System Solution compared to System per Die Type Solution

Table 2: Relative throughput as a function of circuits per carrier and wafer exchange time.

B. Impact of # of Die Types & Counts per Circuit

The impact of the number of unique die types per circuit, and the quantity of each die type on the relative throughput of each solution type was also analyzed. This analysis was done for a fixed number of 28 circuits per carrier and a 30-second wafer + tooling exchange time.

As can be seen in Table 2, a Dual Table system, on average, doubles the relative throughput of a Single Cell per circuit solution. Generally, the placement speed doubles, and the time spent exchanging wafers + tooling is cut in half, resulting in this improvement. The Single and Dual Table Single System per Circuit solutions exhibits a 60% to 90% improvement in throughput in this example.

Secondly, the overall variation from 2 to 4 to 8 unique device types has much less impact than the number of circuits per carrier noted in Table 1.

Finally, the relative quantity of each unique die type has a more significant impact than the number of unique die types, mainly due to a greater impact on the total number of die on the circuit. (Figure 5)

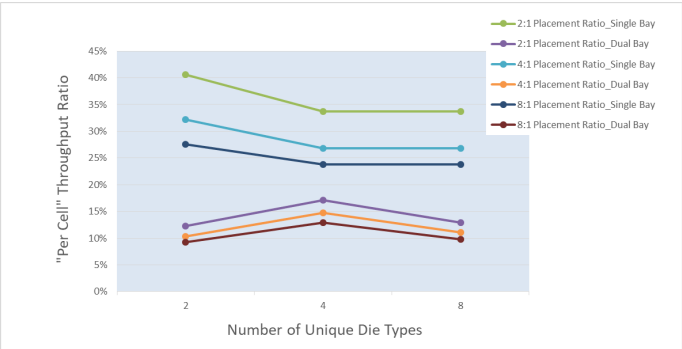

Figure 5: Relative Throughput as a function of the Number of Unique Die types and Quantity per Die type

III. Economic Model Summary

An economic model was created to assess the economic impacts of yield, depreciation per circuit, OPEX, and utilization. Pricing for a single wafer table Single System per Circuit solution was arbitrarily set to $1mil. The price per machine for the single dedicated system per die type solution was set at $500k.

	Single System Single Bay	Multi System Alternative	Comment
"Per Cell" Throughput efficiency	100%	24%	Throughput efficiency of single cell vs multi-cell
Circuits per Year	1273799	1214458	Input number of Assemblies / year
Solution Price	$1,000,000	$2,000,000	Input solution price to meet Assemblies/ year need
Depreciation Years	5	5	Input # of years to depreciate asset Note: a more flexible tool may justify longer depreciation cycle)
Base Depreciation per Unit	$0.157	$0.329	Calculation based on depreciation time interval
COGS of each Assembly	$50.00	$50.00	Input total COGS of all devices being picked and placed + substrate
Throw Rate %	0.13%	0.13%	Input expected device scrap (throw) rate due to mispick
Circuit Yield Loss	0.17%	0.68%	Input expected assembly yield due to misplacements
Total Scrap Cost per Unit produced	$0.150	$0.405	Calculated based on COGS and scrap %
Utilization	85%	60%	Input expected Solution Utilization
Utilization Cost per unit produced	$0.0236	$0.1334	Calculated based on increased depreciation per actual Unit assembled
Operators Required per Shift	1	4	Input # of Operators (1 per system)
Fully Burdened Cost/Oper	$30.00	$30.00	Input Operator Hourly Rate (Fully Burdened)
Operator Cost per Assembly	$0.1413	$0.5929	Calculated based on total operator cost
Floor Space Required	5	20	Input floor area (m2)
Annual Floor Space Cost (incl power, insurance, etc)	$10,000	$10,000	Input total cost per area
Factory Cost per Assembly	$0.0393	$0.1647	Calculated based on total floor space cost
Total Cost per Unit	$0.511	$1.625	
Total Cost if Alternative Solution is free	$0.511	$1.296	

Table 3: Economic Model for HI Assembly

A key observation from the economic model is that, while depreciation cost per assembled circuit is the typical factor used for solution comparison, in reality, the assembly yield has a much larger impact on the overall cost of manufacturing. (Table 3)

For the single bay Single System per Circuit solution, the depreciation cost is only 30.7% of the total assembly cost.

Two other factors heavily influence total assembly cost: total scrap per unit produced and operator cost. Operator cost is assumed to be directly proportional to the number of systems. Based on an estimated increase in defective placements from 100ppm to 400ppm for a four-die HI device, the increased scrap cost for the multi-system solution is more than the depreciation cost for the Single System per Circuit solution.

The economic model shows that even if the multi-system solution is free, the increased scrap, operator, and utilization costs result in the single-system solution delivering a 60% lower overall assembly cost.

III. Conclusion

With the advent of high volume Heterogeneous Integration circuits, efficient advanced packaging assembly solutions are critical to optimizing the overall economics. A comparison of traditional assembly processes, which require a dedicated assembly system per die type, to a novel solution utilizing a single assembly system for all die, demonstrates a 60% cost of assembly advantage for the single-system solution.

Acknowledgment

The author wishes to acknowledge the inventors and patent holders of this novel solution: Mike Yingling, Sean Adams, David Lyndaker & Scott Proctor. ***(Reference #3)***

References

1) IBS. As Chip Design Costs Skyrocket, 3 nm Process Node Is in Jeopardy. 2020. Available online: https://www.extremetech.com/computing/272096-3nm-process-node

2) UCIe 1.0 Specification is an open industry standard developed to establish a ubiquitous interconnect at the package level. Available online: https://www.uciexpress.org/specification

3) High-Speed Wafer Feeder Patent Number: 11164765
Issue date: 11/2/2021
Title: Modular Die Handling System
Inventors: Mike Yingling, Sean Adams, David Lyndaker, Scott Proctor