ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2018 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and electronic assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to engineering topics directly applicable to manufacturing challenges. In every case, the objective is to provide AREA Principals with meaningful results that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a comprehensive website with on-demand content is made available (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals. Longer term reliability evaluation projects may extend into subsequent plan years as needed to complete testing. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities and faculty expertise as needed.

The primary focus for 2018 will be the careful execution of the projects outlined in this document. History indicates that additional topics will be added throughout the year as our capabilities develop, member interests evolve and materials are provided. The research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

MAT1C. Edge Bond and Corner Bond Component Underfills

As the use of minimalist packaging schemes such as wafer level CSP migrates to larger and larger devices, industry interest in component underfill encapsulation for improved thermal cycle reliability is increasing. The use of underfill encapsulation for these board level attachments requires not only selection of the appropriate material but also specification of the extent of underfill required. In many cases, edge bonding and corner bonding may well be adequate. The anticipated benefits of partial encapsulation schemes include reduced process time and materials consumption. Enhanced reworkability is also a likely advantage over full underfill encapsulation given the easier component removal and site dress with partial underfill configurations. This study will compare the effectiveness of reliability enhancement provided by recent industry underfill material offerings when applied to common chip scale packages. Using comparisons to fully underfilled and non-underfilled configurations, the reliability enhancement of various partial underfill approaches will be measured. Previous consortium efforts on this topic have noted improvements in drop shock reliability for essentially all underfill configurations. This study will therefore focus solely on thermal cycle performance.

MAT2D. Pad Cratering Behavior in Cyclic Bend Test by Laminate Material

Several member companies continue to be plagued by pad cratering of laminate materials under critical large components during assembly induced board strains. This project revisits a previously defined consortium test method for comparing pad cratering tendencies among different laminate materials using a cyclic four point bend test. In this vehicle two BGA components are assembled along the axis of board bend in order to impose tensile strains along the outer BGA solder joints which promote laminate pad cratering especially under the corner solder joints. Test traces emanate from the corner joints to allow electrical monitoring of the completed cratering event. In the present study, the pad cratering tendency of several high performance laminates such as Megtron 6 and Nelco 4800 will be compared to our commonly used 370HR laminate material.

MAT4B. Characterization of Heatsink Thermal Interface Materials (TIM2)

This ongoing research program evaluates the performance of various thermal interface materials intended for heat sink applications. Typically candidate materials are suggested by member companies and may include thermal greases, putties, and thermal pads. Using a precision thermal rod test apparatus, thermal resistance is measured as a function of bondline thickness, and where appropriate, heat sink load. The 2018 interface materials list includes several thermal greases (Laird, Nolato, Jones, a few silicone free), thermal putties (Laird, Jones, Allied) and graphite thermal pads (Jones, Panasonic, Allied, Nolato). A select subset of the candidate interface materials will monitored for degradation in TIM2 performance with thermal cycle using a custom FC-PBGA component with a thermal test die. (These will be materials not suited for the capacitance based reliability test method of MAT4C.)

MAT4C. TIM2 Thermal Cycle Reliability

The advertised performance of thermal interface materials for heat sink applications is typically reported as thermal resistance measured in the as-applied state. The stability of this condition may however be suspect, with thermal performance degrading with system operating hours. This project monitors the stability of various member selected TIM2 materials using a capacitance measurement across the TIM bondline. This custom test apparatus mimics the TIM bond to an aluminum heatsink. The prepared thermal interface is stressed in an environmental thermal cycle at individual sites having a range of different distances from the system neutral point. Thermal expansion mismatch between the aluminum heatspreader and the mated circuit board imposes a cyclic shear load on the TIM2 bondlines that can degrade the TIM thermal performance. Using the mathematical analog of capacitance and thermal conductance, the degradation of TIM performance is measured independently at each test site. TIM2 materials have been selected for 2018 evaluation include the silicone based thermal putties Laird T-putty 607, Jones 21-361, and Allied T-Gel SP600.

MAT6 Series: Harsh Environment Electronic Interconnect

As electronics become integrated into higher temperature environments such as those associated with deep well drilling and distributed engine controls in the automotive and aviation applications, higher melting temperature and more thermally stable solder alternatives are being explored. In 2017, our harsh environment electronics thrust will include research on both die level and board level metallic interconnects critical for reliable high temperature electronics applications.

MAT6C. Sintered Silver Die Attach Materials

High temperature die attach materials are critical for the operation of next generation power electronics applications including those using wide band gap semiconductor devices such as SiC. These devices dissipate substantially more energy than conventional electronics. A metal based die attach system is typically required to provide sufficient thermal flux to remove the waste heat from these devices.

Previous AREA research evaluated the sintering characteristics of a candidate sintered silver die attach materials formulated for pressure-less processing. Formulations with either micron scale particles or nanoscale particles were studied. Thermal characterization of the sintered silver bond lines were made with our thermal rod tester. This 2018 continuation project characterizes the strength and thermomechanical stability of similarly constructed sintered silver bonds after intervals of thermal shock stress testing.

MAT6G. Pb-free Solder Alloys for Engine Control Applications

Solders intended to withstand the high operation temperatures such as those encountered in automotive under-the-hood applications (~200˚C) have historically depended on high Pb alloy formulations. The search for Pb-free solder alternatives for these applications and similar aviation engine control applications is on-going. This project examines several candidate Pb-free solder alloys formulated for stability in elevated temperature applications using a twofold approach. Phase 1 (now complete) examined the degradation in solder mechanical properties using arrays of 0603 resistors assembled with the various solder alloy candidates. These assemblies were exposed to extended harsh thermal cycling (-40/150C). Samples were withdrawn at prescribed intervals for device shear testing at room temperature and 125C. Associated microstructural observations are in progress. Phase 2 of this study in 2018 will involve thermal cycle reliability testing of select package types (primarily BTC) assembled with the same solder alloys.

MAT7 Series: Lead-Free Solder Alloy Evaluations

New lead free solder alloys with various alternative alloying elements are being routinely proposed in the industry as replacements (improvements) to the standard SAC305 alloy. Previous AREA results have shown that mechanical and thermal reliability improvements can be correlated to microstructural differences created by varying solder volume and PCB surface finish. Significant effects of solder joint volume and composition on microstructure and thermomechanical performance were observed.

Projects included in this alternate solder alloy thrust include evaluations of microstructure and mechanical properties for various solder alloys and surface finishes. The work encompasses characterizations for both individual solder balls as well as components assembled onto test boards for second level reliability comparisons through thermal cycle or mechanical testing. The performance of the alternative lead free alloy solder joints is often compared to that of the common SAC305 alloy or eutectic SnPb, as appropriate.

MAT7F. Characterization of Low-Melt BiSn Mixed Solder Assemblies

Suppliers of large body BGA components such as microprocessors are promoting the use of low melting point solder for board attachment to minimize the impact of temperature induced warpage on assembly

yield and package reliability. Such suppliers can be expected to supply packages with low melting BGA solder spheres but these special alloy BGA packages are not expected to be universally available by all component suppliers. Board assembly with low melt solder paste will inevitably require mixed solder assembly for some BGA components such as commodity memory parts that will necessarily be sourced with conventional SnAgCu based BGA balls. This project will characterize mixed solder joints formed with various SAC305 BGA spheres joined with BiSn eutectic solder paste. The degree of mixing will depend on the reflow profile and the relative paste to ball volume ratios. Characterization will include microstructural evaluations as well as mechanical property measurements such as local hardness or joint shear strength. Select instances of BiSn mixed solder packages will be subjected to thermal cycle testing for reliability assessment.

MAT8B. Conformal Coating: New Materials and Methods

Conformal coating of circuit board assemblies have long been used for protecting components and circuitry from harsh environmental conditions. While these coatings may mitigate both corrosion failure and Sn whisker shorting risk and protect against other environmental hazards, their impact on thermal fatigue failure rate of board level solder interconnects is not well characterized. The AREA Consortium has been exploring the interconnect reliability consequences of popular conformal coatings since 2013. These studies have examined both SAC305 and SnPb eutectic solder connections with a variety of component types and conformal coating materials. A synthetic rubber coating (Humiseal 1B59U), several EMCAST one part epoxies, a fluorinated Novec material (3M) and a new plasma applied coating have been applied to assembled TB2015 test boards. These coated boards will be subjected to thermal cycle reliability testing in 2018. Using a prior board design will permit direct comparison with previously tested coatings. Uncoated TB2015 boards will be included as control samples.

MAT8D. Conformal Coating for Mitigation of Sulfur Induced Resistor Corrosion

Operating environments with high ambient levels of sulfur are often found in developing countries and in some characteristic industrial settings (e.g., tire manufacturing). Server installations are prone to failures due to corrosion buildup across the top surface of surface mount resistors. While anti-sulfur resistor finishes are now available, too often (through inadvertent or temporarily unavoidable substitution) conventionally finished resistors will still be used on a high reliability server PCBAs. One product protection scheme being considered to mitigate the associated corrosion risk in these instances is a conformal coating of the assembled circuit boards. This project evaluates the effectiveness of several candidate coatings to prevent or slow sulfur induced corrosion on SMD resistors with conventional (not anti-sulfur) finishes. Six different surface mount resistor formats (from 0201 up 2512) have been assembled to test coupons and conformal coated pending corrosion testing in a laboratory Flowers of Sulfur (FoS) test environment. The FoS corrosion test will be run at three different temperatures (in three different member labs) to determine the activation energy of the suppressed corrosion process. Seven different coating materials are queued up for testing, including Humiseal

1B59U, several EMCAST one part epoxies, and a fluorinated Novec material from 3M. Humiseal 2A53, an acrylic formulation used in prior corrosion studies will be included as a reference.

MAT9: Filled Polymer Electrical Interconnects

Conductive adhesives and other filled polymer systems provide an alternate method of electronic interconnect to reflow soldering. Such materials have a long history of use in low cost consumer goods where product design life is relatively short and reliability expectations modest. They typically produce relatively high impedance interconnects, but can nonetheless find application in higher grade electronics where very low assembly temperatures are an absolute necessity. In the fast growing realm of flexible electronics, many candidate substrate materials are incapable of surviving conventional flipchip soldering and therefore require the use of lower temperature electrical attachment technologies such as anisotropic conductive adhesives.

MAT9B. Anisotropic Conductive Adhesive for Low Temperature Die Attach

Flexible electronic applications are typically constructed with flexible polymeric substrates, many of which have very limited temperature capability. Examples include PET, TPU or PEN film substrates. These low cost base materials are not able to survive the temperatures of conventional reflow soldering without damage. Consequently, the joining of flipchip devices to these materials for various wearable or medical applications requires the use of anisotropic conductive adhesives (ACA) to provide both signal and power connections. This study will explore process parameters (time, temperature, pressure) required to produce viable semiconductor die connections on these materials (PET, TPU, PEN). It is anticipated that printed circuitry would often be used in such applications and the die pitch would thus be relatively coarse. Tolerance of the ACA flipchip joints to mild flexural loadings and thermal cycles will be investigated.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. Our Principals often require standardized accelerated life testing for product qualifications. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

REL3E. Effect of Laminate Material on Reliability in Vibration

Consortium experience with harmonic vibration of single component test boards has shown that laminate material selection can affect vibration response of the test board and presumably interconnect fatigue life. This project is intended to be a companion study with the investigation of the role of laminate material in drop shock lifetime. In the case of vibration loading, the mechanical response (*i.e.*, flexural modulus) of the laminate is anticipated to determine the maximum acceleration of the test board at the component site for any given shaker table acceleration. Using mechanically characterized laminate structures, vibration fatigue lives will be measured on boards of various laminate materials for a fixed solder alloy selection. Solder mask defined BGA pads will be used on the test boards to encourage solder joint fatigue failures.

REL5B. PCB Microvia Reliability Screening

Packaging density demands have dramatically increased the use of microvia structures in the PCB designs of our member companies. Many are incorporating these features in their product for the first time and are finding the reliability to be grossly inadequate. Many instances of electrical failures at the base of the microvias are being reported as the board progresses through SMT assembly, that is, circuit boards pass all incoming electrical tests but fail in solder reflow. This is primarily an issue for stacked microvias, especially those with smaller diameters (≤10μm).

This project explores various means of screening unassembled circuit boards for unreliable microvia connections prior to submitting for SMT assembly. These may include various methods of thermal stress exposure and electrical continuity monitoring. While screening product boards may be an option, the preference would be to use manufacturing coupons associated with production PCB panels. Recommendations regarding the preferred attributes of such test coupons would be a desirable outcome. The use of available IPC coupon designs should be explicitly considered to encourage supplier adoption of any recommended screening procedures. Project success will depend critically on the ability of member organizations to supply representative product hardware (good and bad) for evaluation.

REL8A. Wafer Level Chip Scale Package (WLCSP) Interconnect Reliability

The use of wafer level packages in electronic assemblies continues to grow. Often use is motivated by the need for very low profile printed circuit board assemblies. Other times it may simply be a way to reduce packaging costs. While such packages have typically been limited to small die, (<5 mm body), there is interest in expanding the use of these wafer level packaging technologies to larger die. The board level interconnect reliability of larger chip scale packages would of course be suspect. This project will monitor thermal cycle reliability of large body WLCSPs. Larger body CSPs as available (5 – 15 mm) will be used. Stitched devices will be used to monitor interconnect reliability in thermal cycle. If available, fan out wafer level packages may be included.

REL9A. Mixed VIPPO (Via-In-Pad, Plated Over) Array Induced BGA Soldering Defects

The inability to reliably retain solder connections on VIPPO BGA pads through multiple reflows when a PCB design mixes non-VIPPO pads in the same component footprint is now widely recognized as a persistent reliability risk. Liquid metal separation of the BGA joint from the component pad occurs during second reflow above those pads with underlying VIPPO structures. The specific design attributes of mixed VIPPO/non-VIPPO footprints that lead to the BGA joint separations is largely unknown, forcing many to simply eliminate the design flexibility of mixing these two board connection options.

This project explores the BGA solder defect rates associated with various combinations of VIPPO design attributes in the printed circuit board. Assembly test board designs for this experiment have been completed. These designs mix VIPPO and non-VIPPO pads in four different BGA package footprints with a wide variety of different geometric configurations. These test designs will explore the effects of relative VIPPO/non-VIPPO densities, package DNP location, edge proximity. Test components include two standard memory packages as well as 55mm lidded BGA parts, all at 1.0 mm pitch. Boards will be fabricated with select VIPPO locations backdrilled (either shallow or deep) to see if shortening the underlying PTH reduces the reflow induced tensile loading on these VIPPO solder joints. A relatively thick test board (>110 mils) will be used to emulate the behavior of complex network/server applications. Reflow profile attributes will be explored paying particular attention to the temperature gradients produced during second reflow. A key objective of the study will be to identify PCB design rule guidelines for minimizing the occurrence of BGA interfacial separation when using various combinations of board via structures. The test boards used will be sourced with at least two different laminate materials to indicate the contribution of laminate properties on the design rules obtained.

REL9B. Effect of Pad Definition (SMD vs NSMD) on Pb-free Interconnect Reliability

Early studies in the reliability of BGA solder interconnects revealed a marked difference in thermal cycle lifetimes for SnPb eutectic solder joints when solder mask defined (SMD) compared to those that were pad defined. The use of pad defined, or non-solder mask defined (NSMD) was consequently commonly adopted for the PCB footprints of area packages. This board design practice continued as board assembly manufactured widely transitioned to SnAgCu based Pb-free solders without experimental verification that the performance difference in these designs persisted. Given that the thermal fatigue failure mechanisms observed in SAC solders can be fundamentally different than those in SnPb eutectic, it is reasonable to assume their response to the soldermask defined stress concentration at the base of a joint could be different. This study will quantify the reliability consequences of board side pad definition (SMD vs NSMD) for SAC305 BGA joints. It will explore a range of BGA pitches (1.0 to 0.5) and package body sizes, identifying application spaces where SMD board designs may prove acceptable for Pb-free assembly.

REL10B. Effect of Laminate Material on BGA Drop Shock Reliability

Prior AREA research into the drop shock reliability of a BGA208 component often revealed parallel and interactive failure mechanism operative in the laminate material as well as the BGA solder joint. Despite the final electrical failures occurring in the corner solder joints, this parallel laminate crack path was seen to dissipate additional energy during the repetitive drop shock events. Moreover, it contributed to deflection of the ultimate solder joint crack, extending the critical path length. Given the participatory role of the laminate in the failure process, it is hypothesized that laminate material properties (*e.g.*, fracture toughness) can contribute to the measured BGA drop shock reliability. The drop performance of test boards of six different laminate materials will be measured using BGA interconnects of a new high performance solder alloy compared to conventional SAC305 solder. Laminate materials include several high performance (low loss) materials compared to our more commonly used 370HR baseline material.

REL15C. Combined Power Cycle and Environmental Thermal Cycle

Traditional thermal cycle testing of electronic hardware in an environmental chamber is being supplemented with a superimposed constant current power cycle. The intent is to provide a more realistic thermal mechanical reliability stressing through the inclusion of transient temperature gradients similar to those produced in the operation of functional electronics. In some network infrastructure applications, hardware is housed in uncontrolled environments and can therefore experience diurnal thermal cycling with seasonal temperature extremes. A recent interest in the electronics reliability community has been the combination of environmental thermal cycles with mini-power cycles. This test part used for this study is a 45x45 mm laminate BGA package attached to a printed circuit test card. The package contains a 15.4 x 15.8 mm flip chip with a main heater for uniform heating as well as three local individually controllable “hot spot” heaters and five temperature sensors. The BGA solder joints along the package perimeter and those beneath the flip chip comprise five electrical continuity test nets to be monitored for BGA failure during the combined cycling. The APL custom designed power cycle test circuit is used to supply a constant current that drives the main chip heater at the time intervals of interest. It further monitors for short duration resistance ‘events’ and records analog voltage drop on each net to monitor changes in the net resistance, providing a comprehensive failure detection system for every part on test.

Sixteen PBGA modules have been under test using an environmental thermal cycle of -40 to 90 C, (135 minute period) and a superimposed +30 C power cycle (15 minute period), the oldest of which have accumulated >26,000 power cycles and >4000 thermal cycles. Testing will continue through 2018.

REL18A. Electromigration Behavior of BiSn based Solder Joints

Warpage of BGA packages at Pb-free assembly temperatures poses significant assembly challenges for high end server and storage applications. With large body components such as hybrid BGA sockets, temperature induced distortion is particularly challenging and is driving the serious consideration of low

melting BiSn solder assembly for complex server boards. Given that BGA sockets are often used to engage higher power CPU and GPU devices on these server boards, the board attachment solder joints would be required to run at relatively high current levels for extended periods. Lack of an accepted electromigration model for the BiSn system currently inhibits industry adoption of low melt solders for such high current BGA applications. This experimental effort will characterize electromigration void formation and failure rates in BiSn eutectic and BiSn mixed alloy BGA scale solder joints. Measurements will be made as a function of current density and temperature.

REL19A. Event Detection vs Resistance Monitoring for Underfilled Component Failures

The AREA consortium continually seeks out best practices for realistic (product like) reliability evaluations. A longstanding challenge in the thermal cycle testing of underfilled components is accurately identifying the times of individual interconnect failures. Standard testing practice calls for event detection on electrical continuity nets through the board attachment solder joints. The presence of underfill encapsulant however maintains these solder joints in compression and can therefore suppress the event signals associated with solder joint thermal fatigue cracking. A better approach may be to monitor any drift in the total net resistance over time. This project will use our internally developed cyclic test monitor circuit to simultaneously monitor net resistance and electrical events for various underfill test components. Results from these two approaches will be directly compared.

Assembly Process Development

By virtue of its access to surface mount manufacturing equipment, the AREA consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy and quick access in addition to the final project reports (http://www.uic-apl.com/databases).

APD2B. Thin Die Flipchip Assembly

Initial efforts at thin die joining using 60μm thick die with conventional flux dip and convection reflow has clearly demonstrated the challenges of die warpage. Die bump contact to the substrate cannot be reliably maintained through the reflow process; mechanical hold down is required. The incorporation of a new Finetech Pico bonder into the APL tool set now allows a systematic assessment of thermocompression bonding parameters for such thin die. Flipchip thermocompression bonding

process definition will begin with moderately thin (300μm) die with perimeter bumps bonded to flexible substrates such as polyimide or PEN. Subsequent test die will be sourced with progressively thinner silicon, perhaps 150μm or 100μm. Laser joining will also be explored using a transparent quartz hold down plate.

APD8A. In-line Vacuum Reflow: SMT Process and Reliability

Solder void formation in paste reflow assembly processes has been a persistent industry problem especially for components requiring larger soldered areas such as QFNs with central thermal pads. Voided solder in these connections translates into reliability risks for higher power devices where the heat flux through the solder connection is critical to continued device function. Solder process voids inconveniently located directly at die hot spot locations can be particularly damaging, often leading to device failures. New SMT reflow oven designs with in-line vacuum chambers in the high temperature reflow zone are now being offered to the industry as a robust solution to this assembly challenge. This project will explore the process parameters required to minimize solder voids using an in-line vacuum reflow oven. Select examples of assembled packages will be used to compare interconnect reliability between voided and un-voided solder joints.

APD11B. Laser Selective Reflow Applications for Electronic Assembly

A developmental area laser selective reflow (aLSR) tool designed for flip chip solder attachment has been provided to the APL for alternate exploratory assembly work. In the tool's intended application, a near uniform area beam impinging of the back of a silicon die produces a relatively uniform heat under the die to reflow die bumps to a substrate. Laser reflow for other board level surface mount assembly operations is less straightforward. The local reflow conditions at each component are unique, dictated by the physical attributes of the component (thermal mass, thickness, area, and emissivity). Alternate laser reflow applications are all situationally dependent and must be experimentally examined on a case by case basis. This project will explore a wide range of potential solder reflow applications that could benefit from the local and 'programmable' nature of an aLSR process. Anticipated applications include die stack joining, flex cable solder attachments, plated solder bump reshaping and local attachment of passive devices (e.g., with alternate solders). Instances where reflow temperatures must be shielded from nearby temperature sensitive devices such as optoelectronic assemblies or on-board battery sensors will be solicited for trial. Test hardware and assembly process suggestions from the membership are welcome.

APD11C. Laser Rework Applications and Process

The local nature of the laser reflow process naturally lends itself to assembly rework which necessarily requires a highly localized and controlled reflow environment. Planned APL access to a custom laser rework tool mid-year 2018 will enable a range of potential rework applications. A full range of board

level component removal and replacements will be attempted including passive devices as well as a variety of active device packages. Rework of components on conformally coated printed circuit assemblies may be possible as well. Member company suggestions and hardware contributions are welcome.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and useful manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager and staff will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Project needs may require the AREA staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.