Dear Members,

AREA Consortium research continues to influence the industry on many topics. Our impact at the recent SMTA International technical conference is a prime illustration. SMTAi is a key forum for the electronics manufacturing industry to share new understanding and experimental observations and our work was on prominent display in SMTAi 2017. At the dedicated AREA Consortium session we repackaged a bit of the technical content that we've shared with you privately in prior years to entice your industry brethren to participate in our AREA collaborative research. Our first two papers were presented by two of our long time member representatives, Lars Bruno and Richard Coyle. For the third paper we called on our award winning graduate research assistant, Mohommed Genanu (2016 Best Student Paper) to discuss microstructural consequences of a laser reflow soldering process. Moreover, at least three of our member companies chose to share some consortium research content they found pertinent to topics they were presenting outside of our session.

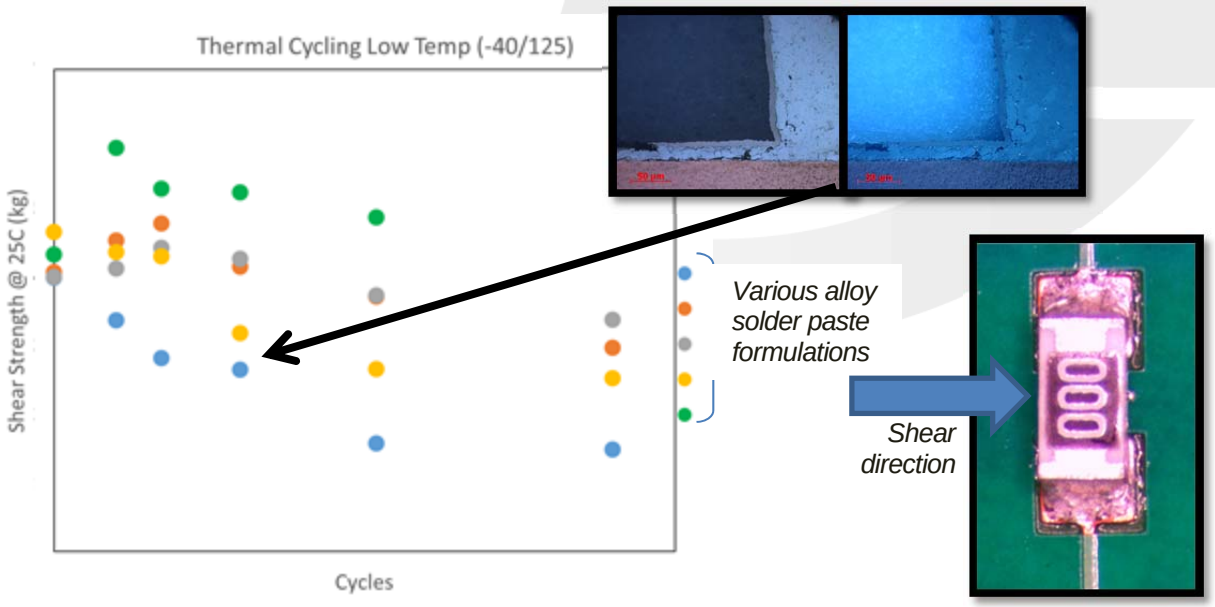
Clearly, there's relevant work going on here in the AREA research portfolio. Spread the word.

Sincerely,

Jim Wilcox

Consortium Manager

MAT6G. Pb-free Solder Alloys for Engine Control Applications



The long term mechanical stability of several solder alloys designated for extended elevated operation is being evaluated by monitoring the shear strength of 0603 resistor solder joints through various harsh environmental cycles. All samples in the -40/125C and -40/175C chambers have been removed for test save one set (now at ~3000 cycles). The -40/150C cell has two sample sets still cycling. Shear strength measurements at room temperature and high temperature are complete for the removed samples. Cross sections of all of the samples removed have been made and microstructural analysis is ongoing. High quality optical images to be used in determining desirable or interesting sites for subsequent electron microscopy analysis will be finished soon. EBSD analysis will be done on a select few to quantify the Sn grain recrystallization processes known to precede thermal fatigue damage

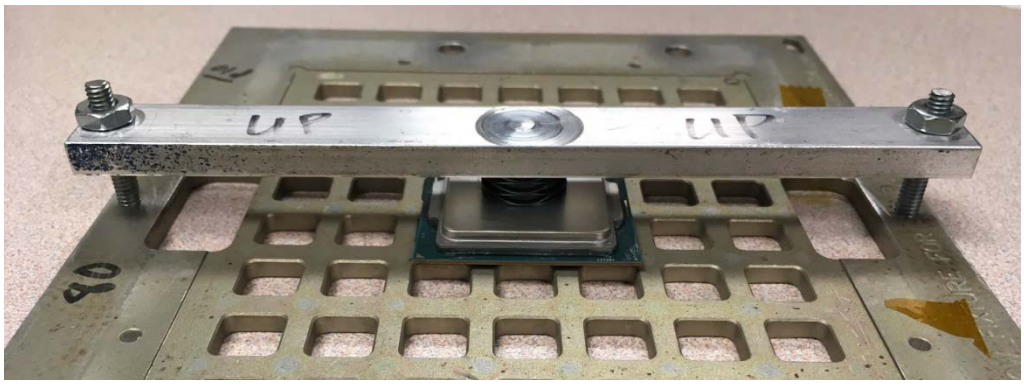
MAT4D. High Performance Die Level Thermal Interface Materials

Die level thermal interface materials are used to provide an enhanced thermal path between underfilled flipchips and a topside metal heat spreader. These materials are often referred to as a TIM1 in reference to their first level packaging role. Because of the strong mechanical coupling from the chip underfill, a large mismatch between the coefficients of thermal expansion of the chip and substrate can result in significant warpage. The attached chip is essentially flat (stress free) at the underfill cure temperature, typically 125 to 150°C. Cooling through the Tg of the underfill (typically 100 to 120°C) after cure, produces increasing chip warpage as the temperature decreases. In order to manage these thermomechanical stresses and accommodate chip curvature, a very important property for a TIM1 besides thermal conductivity is mechanical compliance; a function of bond line thickness, modulus of elasticity and flow stress. In the pursuit of the very low thermal resistance of <10°C mm^2/W for a TIM1 solution, bond lines are reduced, higher filler loadings are used in polymer based TIMs or metallic materials are used. All of these trends decrease mechanical compliance. Delivering a TIM1 with both exceptional thermal performance and sufficient thermal mechanical compliance that does not adversely impact the structural integrity of the chip is a significant technical challenge.

Intel Core i3 processor with thermo-couple embedded in the lid

A study is being conducted of high performance TIM1 candidates, all of which are expected to have thermal resistance well below 10°C mm^2/W. The candidates include two commercially available solutions, indium solder and a silicone gel, and two experimental candidates developed under the DARPA Nano Thermal Interfaces Project: copper nano-spring bonding and carbon nanotubes. Additionally, GaInSn eutectic ternary liquid metal is included in the study. Being a liquid, it offers mechanical compliance and being a metal, very high thermal conductivity. These five TIM1 solutions are used to build two thermal test vehicles: 1.) an instrumented thermal test chip on laminate and 2.) Intel Core i3 processor modules.

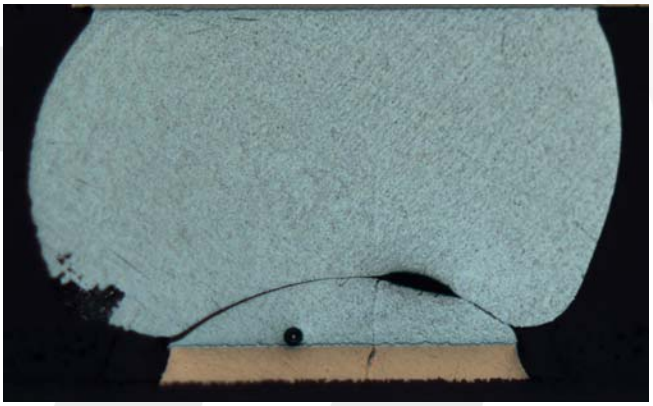
Some early results are in. Using the silicone gel, the Intel Core i3 processor experienced a 4°C drop in core temperature compared to the as-received thermal solution for the same power. The GaInSn liquid metal TIM1 applied to the Intel Core i3 resulted in a 9°C drop in core temperature compared to the as-received thermal solution for the same power. Work still pending includes building the thermal test vehicles and Intel Core i3 modules with indium preforms and copper nano-springs for which material samples have been received. The carbon nanotube material sample has not yet been received.



Fixture for curing TIM1 under controlled spring load.

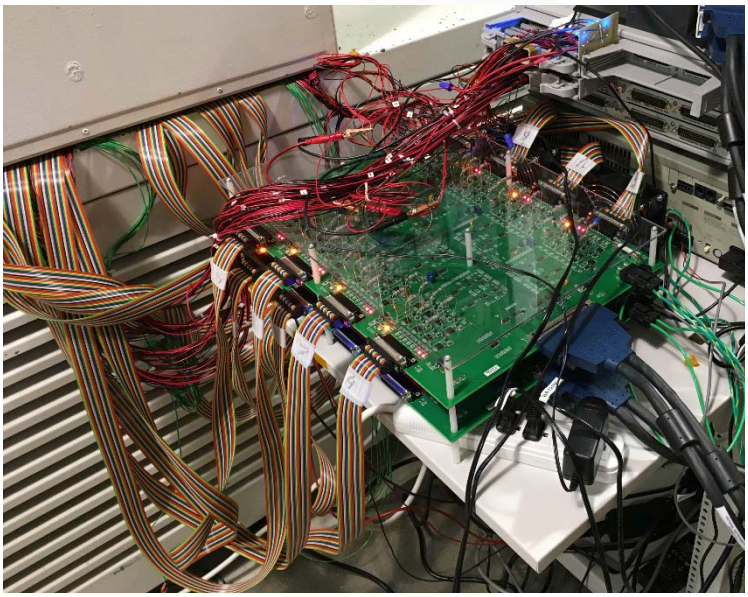
REL15B. Power Cycle Testing

Thermal cycle testing with superimposed power cycles is an ongoing reliability evaluation project. The test program includes three groups of eight flipchip PBGA test modules soldered to individual test cards. The first group has exceeded 2100 thermal cycles (-40 to 90C) and over 13,000 power cycles. These constant current power cycles heat the thermal test chip 30C above the ambient temperature of the thermal cycle chamber. BGA solder joints along the package perimeter and under the flip chip comprise six electrical continuity test nets that are monitored for both short duration "failure events" and long term resistance change. Two tested modules showing both 'events' and significant increases in net resistance have been removed for failure analysis. In both cases, head-in-pillow defects were observed located at the package edge in the failing net. Testing will continue until failure rate distributions are established. A second reference group is being thermal cycled only (without imposed power cycles) in the same chamber. Signs of significant voltage drop across a corner BGA are apparent after 1500 thermal cycles. Testing continues in order to drive failures in the other five stable nets.



Head on Pillow BGA solder defects are the first joints to fall out in combined power and thermal cycle test.

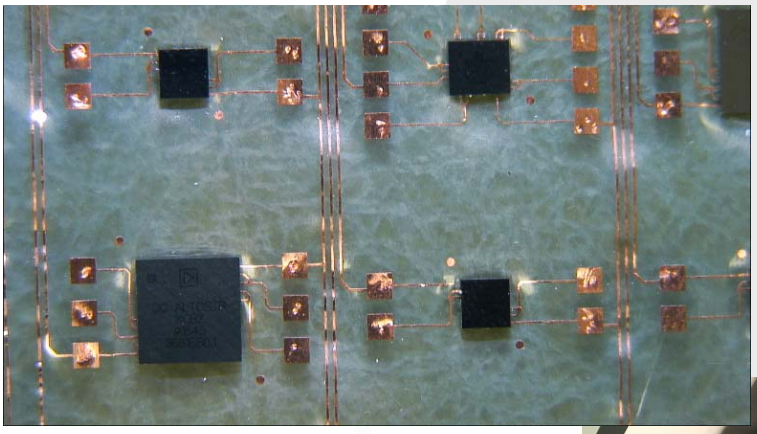
Recently, a third test group has begun cycling and is a replicate of the first group. 250 thermal cycles and 1500 power cycles have accumulated. In order to stress this third group of test modules a second custom, constant current, test circuit board has been added to supply a constant current to drive the main test chip heaters, monitor for failure events and measure DC voltage across every test net. The C# system control code was modified to collect data for groups one and three at the same time, which eliminated the need to duplicate all of the equipment for group three. The same control computer, scanner and power supply are used for first and third test groups. A second NI DAQ and DMM were needed for group three to collect event data and voltage drop data. The photo at left shows the two stacked constant current control boards along with the supporting test equipment used to collect data. Our instrumented power cycle test capacity has been effectively doubled.

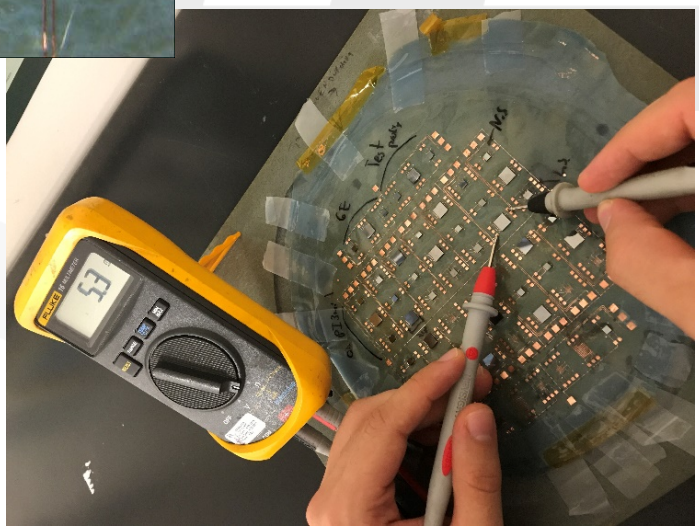


Two internally designed constant current control boards stacked to double the APL power cycle test capacity to 128 channels. Boards shown wired to superimpose power cycles on test boards inside an environmental thermal chamber.

APD11A. Laser Selective Reflow for Thin Die Assembly

A robust manufacturing process for the attachment of components to low cost, temperature sensitive substrates such as PET or TPU will be a key enabling capability for future flexible electronic products. Convection oven reflow soldering processes with isothermal heating (or 'symmetric heating', *i.e.,* same above and below) cannot be used. The peak temperature required for this conventional Pb-free soldering process will damage most such low cost flexible substrate materials. Instead, asymmetric heating processes (*i.e.*, heating solder independently of the substrate) are being actively explored. One such asymmetric heating method, area Laser Selective Reflow (aLSR), is being used to bond wafer level chip scale packaged (WLCSP) devices onto to temperature sensitive flexible substrates. Substrate materials listed in the table below … Flip chip soldering to several substrates and metallizations has been explored, such as copper metallized PI, copper metallized TPU, and silver printed PET. WLCSPs directly flip chips soldered to copper metallized TPU film is shown in the accompanying images.





Flexible Substrate Materials	
PI	polyimide
PEN	polyethylene napthalate
PET	polyethylene teraphthalate
TPU	thermoplastic polyurethane

MEMBERS ONLY

Additions to the AREA report archive …

Isothermal Fatigue of High Temperature Solder Joints
by Harry Schoeller

Reliability Assessment and Microstructure Characterization of Cu Pillars Assembled on Si and Glass Substrates
by Mohammed Genanu, Francis Mutuku, Eric Cotts, Scott Pollard, Aric Shorey, Eric Perfecto, Babak Arfaei