AREA Consortium

Dear Members,

Many of our long-standing reliability test cells have been removed from the thermal cycling chambers to make room for new test cells such as our 2017 conformal coating reliability impact study. Not all components have failed in these stopped tests but sometimes we're forced to make arbitrary decisions on when enough is enough. The MLF100 component for instance is proving particularly resilient in our alternate solder alloy comparison study, many hanging on for more than 10,000 cycles of 0/100C accelerated thermal cycles. The LGA676 is another robust package with many surviving the full duration of our thermal cycle reliability test.

Be sure your travel arrangements are made for our upcoming October consortium meeting (October 25th and 26th). We'll be discussing, among other things, System in Package reliability, die level thermal interface materials, and flexible electronic assembly. And, in addition to our usual research project technical updates we've arranged for some guest talks (lectures?) from our faculty partners at Cornell and Auburn Universities. We hope you can join us.

Sincerely,

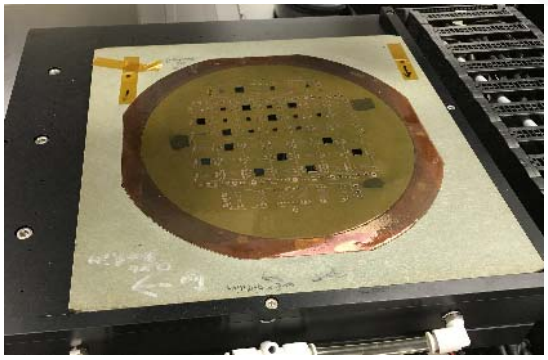
Jim Wilcox

Consortium Manager

MAT7E. Joining for Flexible Hybrid Electronics (FHE)

Joining techniques for attaching semiconductor devices to temperature sensitive flexible substrates are being investigated. Several joining techniques are being considered in our FHE assembly program: conventional convection oven reflow, area laser selective reflow (aLSR), Finetech die bonder, mixed solder assembly with BiSn eutectic paste and SAC405 solder spheres, and Self Assembly Anisotropic Conductive Paste (SAP). The laser reflow process is receiving much of our initial focus.

Our aLSR tool has demonstrated the ability to join various wafer level CSPs to metalized 50 µm thick Kapton (polyimide) substrates (left image). Attributes of the three different wafer level CSPs being joined to polyimide substrates are listed in the table below. All three are bumped with SAC405 solder bumps at the pitches and dimensions indicated. Polyimide is selected as the baseline test vehicle because it is able to withstand the process temperatures of the convection reflow oven thus making direct comparisons possible between novel method solder joints and those made with conventional chip joining processes. Acceptable alternative joining techniques successfully demonstrated on polyimide can then be applied to more temperature sensitive substrates.



Kapton substrate in a holding pallet on a laser reflow table with multiple WLCSPs attached using aLSR

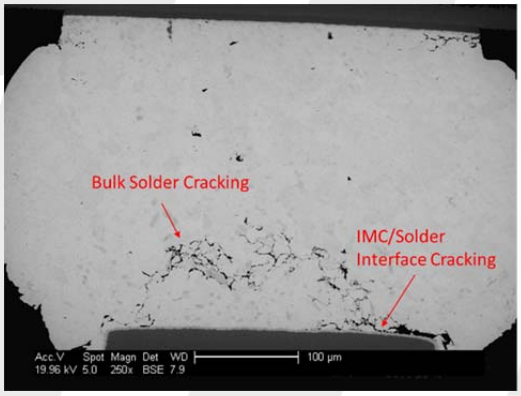
Physical attributes of WLCSP test die used for polyimide aLSR joining experiments

Die Size (mm)	Die Thickness (µm)	Bump Pitch (µm)	Bump Height (µm)
6.05 ×6.13	360	500	240
2.89 ×2.89	378	400	208
3.57 ×3.16	290	350	180

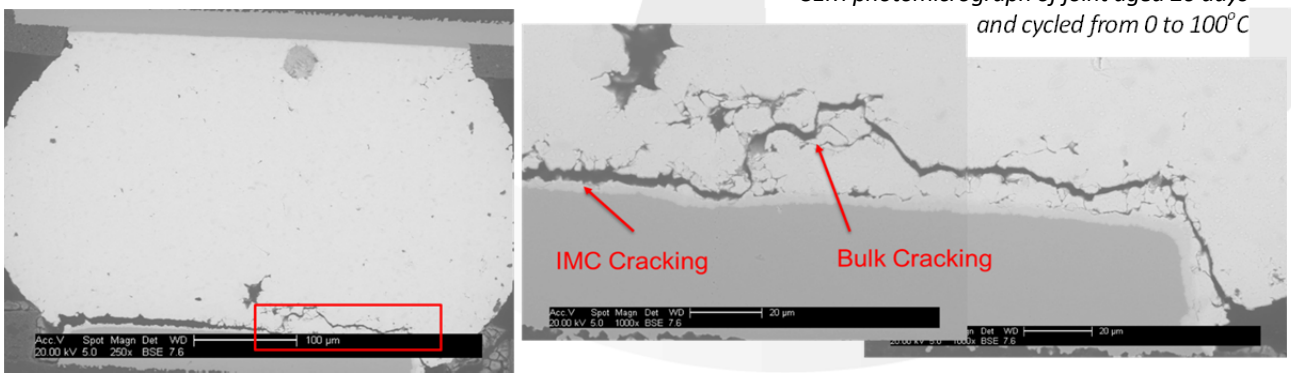
REL7A. SnAgCu Thermal Aging Effects

192 I/O daisy chained CABGAs, joined to a Panasonic R-1755V board with SAC305, were aged for either 0, 20, or 40 days at 125°C prior to thermal cycle reliability testing. Aged assemblies were subjected to either a 0 to 100°C or a -40 to 125°C ATC profile. Contrary to industry expectation, thermal aging at 125 °C was observed to increase cycles to solder joint failure; in the case of 40 day aging increasing the characteristic cyclic lifetime by ~50%

Thermal fatigue failures were observed to occur primarily in corner solder joints. Corner joints are located at largest package DNP and, for the particular large die CABGA packages used, are also aligned with the silicon die corners, so failure at these joints is expected. The observed failure mode however was not the typical Sn recrystallization and solder cracking along the package side of the joint. Instead, the failure was a mixture of bulk solder cracking and IMC/solder interface cracking on the board side of the joints. This atypical failure mode was operative irrespective of thermal aging history. Failure analysis is being conducted to gain insight into the atypical aging response. Possible aging induced changes in the circuit board properties are also being explored.

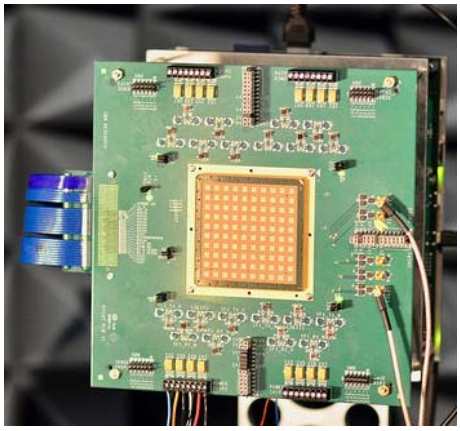


SEM photomicrograph of joint aged 20 days and cycled from 0 to 100°C



SEM photomicrographs of a joint aged 0 days and cycled from 0 to 100°C

REL11B. Effect of Superimposed Tension on BGA ATC Reliability

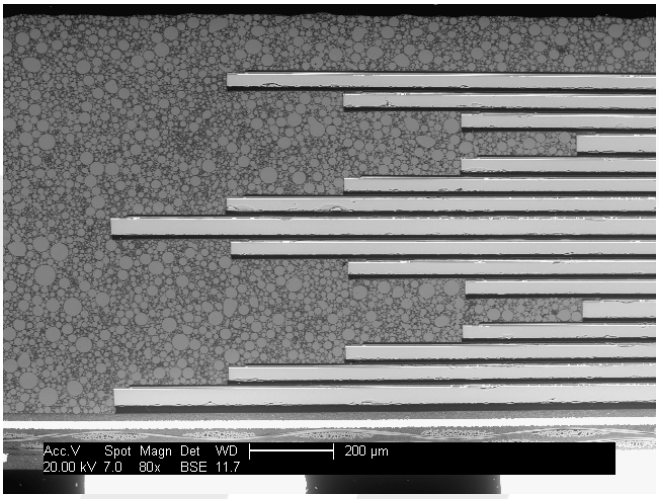


Prototype of silicon mmWave phased array antenna for 5G base stations. – IBM Research

Phased array antennas for 5G cellular networks are now in development. Prototypes of these integrated circuit antennas operate at 28GHz (millimeter waves). Given the requirement for one exposed broadcast surface on these antenna-in-package structures, the thermal solutions required to cool the silicon will be unconventional. One proposal is a thermal interface material applied through an opening in the carrier circuit board. Any applied TIM load would therefore apply tension to the package BGA solder joints. The reliability consequences of these tensile loads are being investigated in this project. Test packages have been joined to windowed circuit boards for the application of simulated TIM loads with concurrent ATC testing.

REL9A. Via in Pad Plated Over (VIPPO) Soldering Defect

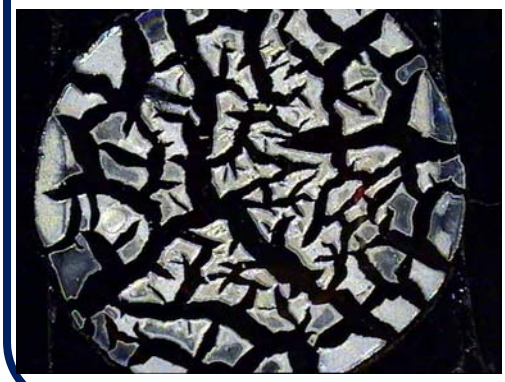
Most of the components that will be used to populate the Mixed VIPPO Test Board have been acquired and are being thoroughly characterized. The test board design attributes are being defined. Our mixed VIPPO population strategy will be shared at the October meeting before the board design is finalized and submitted for fabrication. In the meantime, we are pursuing single-joint experiments to elucidate the formation mechanism for the characteristic second reflow VIPPO solder defect of interest. A new apparatus that provides a constant upward force and that can be used either on a hot stage (for temperature-gradient tests) or inside a box oven (for quasi-isothermal tests) has been designed and is being fabricated. We anticipate using this apparatus with the hot stage of the Finetech bonder as it provides a finer temperature control than a hot plate.



Stacked die profile in a testable NAND memory component that will populate one site on the mixed VIPPO test board

MAT6C. Sintered Silver Die Attach

To better understand the formation and evolution of the gaps inside the latest material with the nanometer-scale silver particles, glass "die" and "substrates" (made from glass microscope slides cut to smaller sizes) were used. These allowed visual observation and video recording of the sintering process. Various heating rates, partial paste drying conditions, glass surface textures, and even a modest amount of pressure were tried. It was seen that at relatively low temperatures, well below the boiling point of the solvent, bubbles formed in the liquid periphery; at only moderately higher temperatures the first gaps appeared and grew while more bubbles formed in the liquid between the gaps. No conditions produced gap-free sintered silver, although some trends were seen in the number and final size of the gaps (unfortunately usually in opposite direction: When the gaps were smaller overall their number was generally larger. Examples of this gap size vs number trade-off is illustrated in the images below. Drying at ambient temperature produces even larger (and fewer) gaps. The previously evaluated material (with micron-scale particles), when sintered between glass slides, remained gap-free.



Nanoparticle silver paste deposits dried for the same amount of time at low T (50C, left) and high T (80C, right).

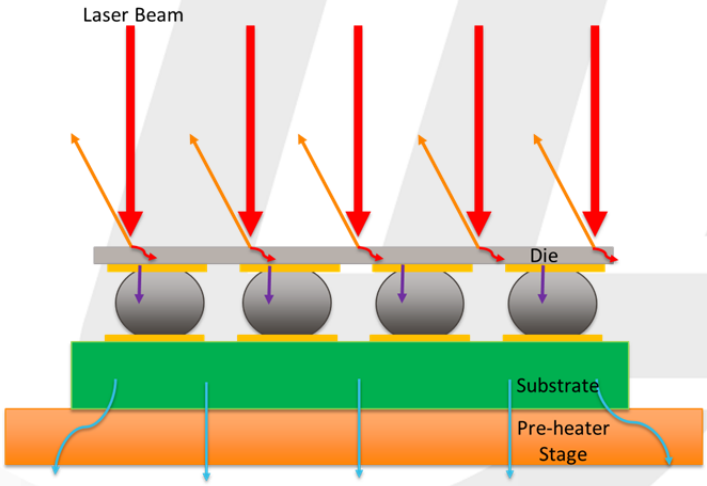
Different paste sample sizes compared at the same scale.

AREA Consortium

APD11A Laser Selective Reflow for Flip Chip Assembly

We have been actively exploring the process characteristics and potential applications of our resident area Selective Laser Reflow tool. For several key applications, we've completed a thorough analysis of the reflow process and thermal distributions. One area of particular interest is the complex heat transfer processes involved in flipchip solder assembly. We have investigated how the silicon die (thickness and metal interconnect layers), solder bump pitch and diameter and substrate material impacts the reflow process. When exposed to infrared laser light, a silicon die will reflect, absorb, and transmit some fraction of the energy impinging upon it. The allocation of the laser energy among these paths is dictated by the thickness of the die, the die metallization layers, and the finish of the backside surface. A die with a highly mirrored surface will reflect more of the energy resulting in a lower amount of energy absorbed and transmitted. Preliminary experiments using identical die with varying degrees of surface polish have shown that the peak temperatures can vary by up to 15°C, with mirrored surfaces being cooler.

The amount of energy transmitted through the silicon in the form of laser light is quite limited for common die thicknesses (*e.g.,* >200 µm) but increases as the die thickness decreases. Much of the laser energy instead converts to heat as it is absorbed in the silicon and then rapidly conducts into the solder bumps to produce local reflow events. The substrate and laser stage are at much lower temperatures than the silicon die and consequently act as a heat sink. Reflow and solidification processes therefore take place under sizeable temperature gradients.



Schematic of laser induced heat flow during aLSR flipchip joining.

It is also important to recognize the role that air is playing in this highly transient process. Air is well recognized as a good thermal insulator and continues to play that role here. This can have significant implications as any air gaps that are present will act as an insulator and prevent any heat dissipation. This can most significantly be seen when a substrate is not flat, resulting in an air gap between the substrate and pre-heating stage. The region of the substrate in contact with the stage will be able to conduct the heat through while the region above the air gap will not, resulting in significantly higher local temperatures and relatively large thermal gradients.

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Additions to the AREA report archive …

Broadband Printing 2: Step Stencil Design Evaluations
by Michael Meilunas

Using Electrical Capacitance and Mechanically Representative Hardware to Evaluate the Thermal Mechanical Stability of Thermal Interface Materials
by Michael Gaynes, Lauren Boston and Andrew Yu