ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2017 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and electronic assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to engineering topics directly applicable to manufacturing challenges. In each case, the objective is to provide AREA Principals with meaningful results that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to their product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a comprehensive website with on-demand content is made available (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals and the AREA Steering Committee. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities as needed.

The primary focus for 2017 will be the careful execution of the projects outlined in this document. History indicates that additional topics will be added throughout the year as our capabilities develop, member interests evolve and materials are provided. The 2017 research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

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Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenges. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

MAT1B. Reworkable Component Underfills

Evaluation of the current sets of capillary underfill encapsulant materials is nearing completion. Materials being evaluated include reworkable offerings from Zymet, Namics, Henkel and HB Fuller. Dispense process definition and reworkability assessment for the first set of materials was completed in an earlier phase of the project. The reliability impact assessment of these materials will however continue to completion in 2017. It includes a comparison of SnPb BGA joints either cleaned or not cleaned prior to underfill, as well as with the SAC versions of the same components underfilled with the same materials. A comparison of two different solder mask materials will be possible as well. Thermal cycle reliability of the TB2015U component set in the as-underfilled state (non-reworked) will be determined for each of these materials. The second set of materials, used to underfill a large BGA on TB2016U, will continue undergoing similar reliability tests. In addition, the rework capability of each will be explicitly explored. Rework evaluations will be done before and after a prescribed thermal cycle exposure which will simulate field return conditions. The process of underfilled component removal and site redress will be exercised prior to examination for damage to the PCB mounting surface.

MAT4B. Characterization of Heatsink Thermal Interface Materials (TIM2)

This ongoing research program evaluates the performance of new thermal putty and grease materials intended for heat sink applications as they come available. Typically candidate materials are suggested by member companies. Using a precision thermal rod test apparatus, thermal resistance is measured as a function of bondline thickness, and where appropriate, heat sink load. A second facet of the project explores the stability of TIM2 performance under environmental thermal cycle in a single component application. Using a custom instrumented FC-PBGA component with a thermal test die, a select subset of the candidate interface materials will monitored for degradation in TIM2 performance with thermal cycle, either through interfacial failure or bulk material 'pump out'.

MAT4C. TIM2 Reliability with Ganged Heat Sinks

For manufacturing convenience (and perhaps improved lateral heat spreading), a common heat sink may be applied across several adjacent but discrete power dissipating devices on a complex circuit board assembly. Thermal expansion mismatch between the common (or ganged) heat sink and the underlying circuit board imposes an additional global cyclic shear load on the TIM2 bondlines that can accelerate degradation of the TIM thermal performance over that observed on a single component heat sink application. This project constructs an apparatus to monitor the capacitance across the dielectric TIM2 bondlines of discrete components having a shared aluminum heat spreader as the assembly is exposed to environmental thermal cycles. Using the mathematical analog of capacitance and thermal conductance, the degradation of TIM performance is measured independently at each component. Four TIM2 materials have been selected for the initial evaluation: Chomerics Gel 30, Laird T-Putty 508, Jones 21-340E-LF2, and Timtronics sil-free 5W.

MAT4D. High Performance Die Level Thermal Interface Materials (TIM1)

Materials designed to efficiently conduct heat directly from the backside of semiconductor die to metal heat spreaders are referred to as first level thermal interface materials (or TIM1). These materials must accommodate very thin bondlines and the cyclic pumping action imposed by thermal cycle induced package warpage. Several high performance TIM1 materials, including silicone gels, putties and greases, liquid metal (GaInSn), reflowed indium and possibly some experimental z-compliant carbon nanotube materials will be evaluated in this study. The baseline thermal resistance of each material will be measured using a thermal rod tester. The stability of the thermal performance of these materials will be measured in thermal cycle using an instrumented first level thermal test vehicle. This thermal TV includes resistive heating test die and embedded thermocouples in the heatspreader above the die.

MAT5B. Solder Paste Voiding Characteristics

Solder paste voiding has become a point of industry concern for the soldering of QFN thermal pads. Ill placed voids under a QFN thermal can lead to local hot spots and component failure. Consequently, paste suppliers have been under pressure to develop lower voiding paste formulations. This project examines the baseline voiding behavior for various paste materials. Voiding levels in QFN pad areas will be compared to those in the I/O leads. Other reflow oven process parameters will also be considered.

MAT6 Series: Harsh Environment Electronic Interconnect Research

As electronics become integrated into higher temperature environments such as those associated with deep well drilling and distributed engine controls in the automotive and aviation applications, higher melting temperature and more thermally stable solder alternatives are being explored. In 2017, our harsh environment electronics thrust will include research on both die level and board level metallic interconnects critical for reliable high temperature electronics applications.

MAT6C. Sintered Silver Die Attach Materials

High temperature die attach materials are critical for the operation of next generation power electronics applications including those using wide band gap semiconductor devices such as SiC. These products dissipate substantially more energy than conventional electronics. A metal based die attach system is typically required to provide sufficient thermal flux to remove the waste heat from these devices. Previous AREA research evaluated candidate sintered silver die attach materials having micron scale silver particles and formulated for pressure-less processing. This latest project will include at least one silver paste formulated with nanoscale particles. The dramatically smaller particle size provides a more reactive system expected to lower the processing temperatures. The project scope includes optimization of the sintering process and characterization of the resulting microstructure, joint strength and thermal stability. Later in the project, detailed thermal characterization measurements will be made, subject to the resolution limits of the conduction measurement apparatus.

MAT6G. Pb-free Solder Alloys for Engine Control Applications

Solders intended to withstand the high operation temperatures such as those encountered in automotive under-the-hood applications (~200˚C) have historically depended on high Pb alloy formulations. The search for Pb-free solder alternatives for these applications and similar aviation engine control applications is on-going. This project examines the degradation in mechanical properties of several candidate Pb-free solder alloys formulated for stability in elevated temperature applications. The approach will be to use arrays of 0603 resistors assembled with these latest next generation solder alloy candidates. The assemblies will be exposed to extended harsh thermal cycling (-40/125C and perhaps more extreme -40/150C). Samples will be withdrawn the chamber at prescribed intervals for mechanical testing with a device shear test at room temperature and 125C. Any observed degradation in mechanical strength of the alloys or interfaces will be correlated with microstructural observations.

MAT7 Series: Lead-Free Solder Alloy Evaluations

New lead free solder alloys with various alternative alloying elements are being routinely evaluated by the industry as replacements (improvements) to the standard SAC305 alloy. Previous AREA results have shown that mechanical and thermal reliability improvements can be correlated to microstructural differences created by varying solder volume and PCB surface finish. Significant effects of solder joint volume and composition on microstructure and thermomechanical performance was observed.

Projects included in this alternate solder alloy thrust include evaluations of microstructure and mechanical properties for various solder alloys and surface finishes. The work encompasses characterizations for both individual solder balls as well as components assembled onto test boards for true second level reliability comparisons through thermal cycle or mechanical testing. The performance of the new lead free alloy solder joints will be compared to that of the common SAC305 and SnPb alloys as appropriate.

MAT7E. Surface Finish and Solder Volume Effects on Thermal Cycle Reliability

The microstructure of lead-free solder alloys is well known to be affected by solder joint volume and composition and that the microstructure in turn greatly affects the reliability of the solder interconnects. This project has been exploring the effect of PCB surface finish on microstructure and reliability of BGA and LGA package interconnects in various accelerated thermal cycles (-40/125°C, 0/100°C and 20/80°C). Investigation of the effect of PCB surface finish (Cu-OSP vs. ENIG) and solder volume on the Sn grain morphology in various commercial components is well underway. Many test cells have now completed but several still await completion of thermal cycle stress. The ATC performance of various candidate alloys (such as Innolot, Violet, and two other alloys microalloyed with Bi and Sb) are being compared to SAC305, SAC 105 as well as eutectic SnPb solder. A considerable amount of microstructural analysis on as-assembled samples and failed samples has been completed. Project will continue to completion. With the exception of some 20/80°C test cells, ATC testing and analysis is expected to complete in 2017.

MAT7F. Thermal Cycle Reliability of Pb-free Mixed Solder Assemblies

AREA consortium studies of alternate Pb-free solder alloys intended for improved reliability performance at more extreme operating environments such as at elevated temperatures have been underway for several years. These new solder alloys typically derive their improved long term stability through increased dependance on solid solution strengthing with alloying elements such as Bi or Sb. Our previous evaluations of these candidate alloys were performed with homogeneous BGA solder connections to the board, meaning the composition of the assembly solder paste matched the composition of the component solder ball preform. This approach quantifies the ultimate reliability benefit of a complete conversion to any of these candidate alloys. The reality of the industrial supply chain however would dramatically limit the available of components with such novel BGA ball compositions. Conversion to a new solid solution strengthened solder alloy paste would instead almost certainly require instances where it would be used to attach now conventional SAC305 BGA components. This project will explore the mixed alloy reliability consequences of several new solid solution hardened Pb-free solder paste formulations when used with SAC305 BGA balls.

MAT8B. Conformal Coating: New Materials and Methods

Conformal coating of circuit board assemblies have long been used for protecting components and circuitry from harsh environmental conditions. While these coatings may serve to mitigate both corrosion failure and Sn whisker shorting risk, their impact on other reliability failure risks such as thermal fatigue of solder interconnects is not well characterized. The AREA Consortium has been exploring the interconnect reliability consequences of popular conformal coatings since 2013. These studies have examined both SAC305 and SnPb eutectic solder connections with a variety of component types and conformal coating materials. In 2017, a synthetic rubber coating (Humiseal 1B59U), several

EMCAST one part epoxies, a fluorinated Novec material (3M) and a new plasma applied coating will all be applied to assembled TB2015 boards for thermal cycle reliability testing. Using the prior board design will permit direct comparison with previously tested coatings. Uncoated TB2015 boards will be included as control samples.

MAT8D. Conformal Coating for Mitigation of Sulfur Induced Resistor Corrosion

Operating environments with high ambient levels of sulfur are often found in developing countries and in some characteristic industrial settings (e.g., tire manufacturing). Server installations are prone to failures due to corrosion buildup across the top surface of surface mount resistors. While anti-sulfur resistor finishes are now available, too often (through inadvertent or temporarily unavoidable substitution) conventionally finished resistors will be used on a high reliability server PCBAs. One product protection scheme being actively considered is mitigate the associated corrosion risk is the use of conformal coating on server boards. This project evaluates the effectiveness of several candidate coatings to prevent or slow sulfur induced corrosion on SMD resistor with conventional (not anti-sulfur) finishes. Six different surface mount resistor formats (from 0201 up 2512) will be assembled with a no-clean solder paste and conformal coated before being subjected to a laboratory Flowers of Sulfur (FoS) test environment. The FoS corrosion test will be run at two different temperature to determine the activation energy of the corrosion process. Up to eight different coating materials will be tested. Under consideration for inclusion are: Humiseal 1B59U, several EMCAST one part epoxies, and a fluorinated Novec material from 3M. Humiseal 2A53, an acrylic formulation used in prior corrosion studies, will be included as a reference.

MAT9: Filled Polymer Electrical Interconnects

Conductive adhesives and other filled polymer systems provide an alternate method of electronic interconnect to reflow soldering. Such materials have a long history of use in low cost consumer goods where product design life is relatively short and reliability expectations modest. They typically produce relatively high impedance interconnects, but can nonetheless find application in higher grade electronics where very low assembly temperatures are an absolute necessity. In the fast growing realm of flexible electronics, many candidate substrate materials are incapable of surviving conventional flipchip soldering and therefore require the use lower temperature electrical attachment technologies such as anisotropic conductive adhesives.

MAT9B. Anisotropic Conductive Adhesive for Low Temperature Die Attach

Flexible electronic applications are typically constructed with flexible polymeric substrates, many of which have very limited temperature capability. Examples would include PET, TPU or PEN film substrates. These base materials are not able to survive the temperatures of reflow soldering without damage. Consequently, the joining of flipchip devices to these materials for various wearable or medical applications requires the use of anisotropic conductive adhesives (ACA) to provide both signal and

power connections. This study will explore process parameters (time, temperature, pressure) required to produce viable semiconductor die connections on these materials (PET, TPU, PEN). It is anticipated that printed circuitry would be used in such application and the die pitch may thus be relatively coarse. Tolerance of the ACA flipchip joints to mild flexural loadings and thermal cycles will be investigated.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. Our Principals often require standardized accelerated life testing for product qualifications. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

REL3D. Elevated Temperature Harmonic Vibration

Apparatus, instrumentation and procedures for harmonic vibration testing in the APL were developed through earlier consortium efforts. For uniformity of mechanical loading on the solder joints of interest, a single component test board is used with centrally located CABGA256 package. Vibration loading can be run at an acceleration (G) level of choice with or without tracking of the test board resonant frequency. An oven has been mounted above the shaker table to enable elevated temperature vibration testing. Procedures for elevated temperature testing will be defined using SAC305 BGA solder connections.

REL3E. Effect of Laminate Material on Reliability in Vibration

Consortium experience with harmonic vibration of single component test boards has shown that laminate material selection can affect vibration response of the test board and presumably interconnect fatigue life. This project is intended to be a companion study with the investigation of the role of laminate material in drop shock lifetime. In the case of vibration loading, the mechanical response (*i.e.*, flexural modulus) of the laminate is anticipated to determine the maximum acceleration of the test board at the component site for any given shaker table acceleration. Using mechanically characterized laminate structures, vibration fatigue lives will be measured on boards of various laminate materials for a fixed solder alloy selection. Solder mask defined BGA pads will be used on the test boards to encourage solder joint fatigue failures.

REL8A. Wafer Level Package Interconnect Reliability

The use of wafer level packages (WLPs) in electronic assemblies continues to grow. Often use is motivated by the need for very low profile printed circuit board assemblies. Other times it may simply be a way to reduce packaging costs. Consistent with their ubiquitous use in current electronic assemblies, wafer level packages will be included on various consortium reliability test vehicles where convenient. Stitched devices (0.35 mm to 0.5 mm pitch) will be used to monitor interconnect reliability in thermal cycle. Preference will be given to larger body WLPs when available, especially those >5 mm.

REL9A. Mixed VIPPO (Via-In-Pad, Plated Over) Array Induced BGA Soldering Defects

Several AREA consortium Principals have reported problems with the inability to reliably form BGA solder connections on VIPPO pads when they're mixed with non-VIPPO pads in the same component footprint. Specifically, liquid metal separation of the BGA joint from the component pad is observed during second reflow above those card pads with underlying VIPPO structures. The specific design attributes of such mixed VIPPO/non-VIPPO footprints that lead to the BGA joint separations is largely unknown.

This project will explore the BGA solder defect rates associated with various combinations of VIPPO design attributes in the printed circuit board. Features considered will include PTH dimensions, VIPPO positions relative to non-VIPPO pads, pad size, via pitch, and component stiffness. PCB laminate CTE and temperature induced warpage are expected be important. At least one relatively thick test board (>110 mils) will be used to emulate the behavior of complex network/server applications. Reflow profile attributes will be explored paying particular attention to the temperature gradients produced during second reflow. A key objective of the study will be to identify PCB design rule guidelines for minimizing the occurrence of BGA interfacial separation when using various combinations of board via structures. The test boards used will be sourced with at least two different laminate materials to indicate the contribution of laminate properties on the design rules obtained. Follow-on investigations of other common via structures such as blind or buried via is anticipated.

REL10B. Effect of Laminate Material on BGA Drop Shock Reliability

In prior AREA research into the drop shock reliability of a BGA208 component, careful failure analysis revealed a parallel and interactive failure mechanism operative in the underlying laminate material. Despite the ultimate interconnect failures occuring in the corner BGA solder joints, this parallel laminate crack path was seen to dissipate additional energy during the repetitive drop shock events. Moreover, it contributed to deflection of the solder joint crack that produced the component electrical failure, extending the critical path length. Given the participatory role of the laminate in the failure process, it is hypothesized that laminate material properties (*e.g.*, fracture toughness) can contribute to the measured BGA drop shock reliability. Through drop testing of BGA interconnections on various laminate substrate materials with differing mechanical response, the magnitude of this effect will be explored.

REL11B. Effect of Superimposed Tension on BGA ATC Reliability

The effectiveness of thermal interface materials typically improves under compressive load. Consequently, many product thermal solutions require the sustained application of load to the heat sink through a spring loaded fixture. Previous consortium studies have revealed the impact of such sustained loading on the reliability of the underlying package BGA joints, in many instances increasing the cycles to failure. Recent proposals for the cooling of BGA packages with bottom side die require the TIM compressive load be applied against the die up through an opening the circuit board requiring a tensile load on the perimeter rows of BGA solder joints. This study will similarly measure the reliability impact of such a sustained tensile load on the thermal cycle reliability of SAC305 BGA solder joints.

REL12A. Fine Pitch Cu Pillar Interconnect for 2.5D Packaging

2.5D packaging integration technologies (multiple die on a common interposer) are seeing increasing adoption in various sectors of the electronics industry. While these technologies have been convincingly demonstrated by several firms using silicon based interposers, the improved electrical properties and reduced cost of glass interposers are proving increasingly attractive to designers. A collaborative project with several key industrial partners studying ultra-fine pitch metallurgical interconnects between silicon die and glass interposer is in progress. Silicon wafers bumped with solder capped fine pitch copper pillars, have been diced and assembled to circuitized glass interposers. Metallurgical analyses are being performed on the resulting copper pillar joints of varying sizes and pitches down to 50 μm. Of interest are the interfacial intermetallic formation, the second phase particle distribution and the associated solder shear strength in these fine scale joints. The thermal cycle reliability of these various copper pillar interconnect configurations, both underfilled and non-underfilled, is being investigated. The reliability performance on silicon interposers will be compared to that on high and low CTE glass interposers.

REL12B. Joining Cu Pillar Interconnects with Laser Selective Reflow

Recently developed optics that allow the defocusing of an IR laser beam into larger (rectangular) areas of relatively uniform intensity have led to the development of a laser selective reflow tool specifically for flip chip solder attachment. This study is a comprehensive comparison of flip chip attachments formed using laser selective reflow versus those formed with mass reflow in a conventional forced convection oven. The study will include two case studies: Case 1. Mobile applications (40μm pitch copper pillar interconnect with a small die (0.18x6x6mm) and Case 2. Server applications (120mm pitch copper pillar interconnect with larger die (0.78x20x20mm). Solder joint microstructures in each case will be characterized in considerable detail. The dynamic warpage of the packaged die during simulated subsequent board level reflow will also be compared.

REL13A. Compliant Pin Insertions Strains

Compliant (or press fit) pins are being increasingly used in complex assemblies to avoid the challenges of Pb-free wave soldering with thick printed circuit boards. High speed, microcompliant pin connector designs are also finding application for smaller, high speed cards. The effectiveness of these PTH connections is intimately dependent on the diameter of the drilled hole, the plated copper thickness and the surface finish of the PTH wall. The significant insertion load required to create a tight and reliable compliant pin connection also produces measurable bending strain in the circuit board. These imposed board strains can pose a reliability risk to board level interconnects on nearby soldered components. This project will characterize the bending strain field around press fit pins using member supplied circuit board assemblies with the goal of defining the size of the keepout zone required around press fit connectors to maintain safe assembly strain levels at adjacent components. Of interest will be sensitivities to PTH dimensional attributes and support fixture placement. Finer pitch microcompliant pin designs will be used.

REL15B. Power Cycle Reliability of QFN Packages

Wirebond QFN packages have been fabricated with resistive test die for power cycling evaluations using a previously defined AREA Consortium test method. The package is a single perimeter row 12.0 x 10.5 mm body with a 0.4mm lead pitch. Each die contains eight resistive elements to emulate functional hot spots on a die. Power can be dissipated in a realistic fashion through the soldered thermal pad of the QFN body. Solder interconnect reliability in these QFN package is being monitored during active power cycling of each die with uniform power across the die. Many thousands of power cycles have been accumulated without measureable electrical consequence. Cycling will continue.

REL15C. Combined Power Cycle and Environmental Thermal Cycle

Traditional thermal cycle testing of electronic hardware in an environmental chamber has been supplemented with power cycle testing. The intent of this project is to provide a more realistic approach to thermal mechanical reliability stressing through the inclusion of transient temperature gradients similar to those produced in the field operation of functional electronics. In some field applications, hardware is housed in unconditioned structures and can therefore experience diurnal thermal cycling with seasonal temperature extremes. A recent interest in the electronics reliability community has been the combination of environmental thermal cycles with mini-power cycles. Through collaboration with other industry groups, we have obtained the flipchip PBGA test samples necessary for such work. This test part is a 45x45 mm laminate BGA package attached to a printed circuit test card. The test package contains a 15.4 x 15.8 mm flip chip with a main heater for uniform heating as well as three local individually controllable “hot spot” heaters and five temperature sensors. The BGA solder joints along the package perimeter and those beneath the flip chip comprise five electrical continuity test nets to be monitored for failure during the combined cycling. Our custom designed power cycle test circuit is used to supply a constant current that drives the main chip heater at the time intervals of interest. It further monitors for short duration resistance ‘events’ and records analog

voltage drop on each net to monitor changes in the net resistance, providing a comprehensive failure detection system for every part on test.

Testing of eight such modules has begun using an environmental thermal cycle of -40 to 90 C, (135 minute period) and a +30 C mini power cycle (15 minute period), superimposed asynchronously. The plot below shows the actual chip temperature as measured by on-chip temperature sensor #1 (blue) that is located between the center of the chip and a midpoint of an edge. The red line is the programmed temperature profile for the environmental thermal chamber.

REL16A. Die Size Effects on the Reliability of BGA Package Interconnect

Amkor 192 I/O CABGA packages are being used to measure the effect of silicon die size on board level solder joint reliability. SAC305 BGA interconnects on otherwise identical components were obtained with die sizes of 12, 9.5 and 7.2mm square. In 2016, test board populated with these varying die size packages were subjected to two ATC thermal cycle profiles (0/100°C and -40/125°C). The intent was to reveal die size effects on thermal fatigue acceleration factors. Thermal cycling of these parts is still in progress although early results are confounded by atypical board side fatigue failures in the BGA joints. Further cycling, mechanical characterization and failure analysis will continue in 2017. Predictive model development of the thermal cycle results is planned when the observed failure mode is understood.

REL17A. System in Package Interconnect Reliability – SAC305

The heterogeneous integration of various die and wafer level package types on larger substrates that are subsequently soldered to a motherboard is becoming more common in many sectors. These large sub-assemblies are often integrated to the level of having stand-alone testable function at the package level (hence System in Package). This project will compare the interconnect reliability of a 12x12mm molded CSP package (0.8mm pitch) when positioned on a large laminate (SiP) substrate relative to its conventional placement directly on the motherboard. Placement location of the CSP on the SiP substrate will be considered (edge vs. corner placement). All assembled test structures will be subjected to -40 to 125C thermal cycle with event detection of BGA continuity circuits. The large (SiP) substrate will further include a central large die (20x20mm) to properly emulate the thermomechanical response of the assembled SiP structure during a thermal cycle. The large die will be underfilled but not monitored for electrical failure.

REL17B. System in Package Interconnect Reliability – Alternate Pb-free Alloys

Interest the higher levels of integration offered by SiP architectures extends to those industry sectors operating products in harsher environments that may be motivated to find higher reliability solder alternatives to SAC305 solder. This project explores the intersection of industry interest in adopting alternate Pb-free solder alloys and embracing higher packaging integration. 0.4mm pitch CSP and WLCSP devices with SAC125N and SAC405 balls are joined to a laminate substrate (35x35mm) using

several different alternate alloy solder pastes (including Innolot). The populated substrate is attached to an electrically testable board with conventional BGA interconnect for -40 to 125C thermal cycle evaluation. The reliability performance of the various SiP level mixed alloy solder joints will be compared.

Assembly Process Development

By virtue of its access to surface mount manufacturing equipment, the AREA consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy and quick access in addition to the final project reports (http://www.uic-apl.com/databases).

APD1C. Fine Pitch Solder Paste Screening

In 2016, a substantial effort was begun to evaluate the process limitations of fine pitch solder paste screening for thin, dense PCB assemblies as might be found in handheld consumer electronics. The 0.6 mm thick printing test board design used contains 0.3, 0.35, 0.4 and 0.5 mm pitch CSP footprints and 01005, 03015 and 008004 passive placement sites. The components have been strategically arranged for solder paste printing experiments with a focus on stencil technologies. Stencils used to date include an 80 μm thick fine grain stencil, 50 and 80 micron thick stencils with Nami nanocoating and 50 and 75 μm thick stencils with DEK Nano Ultra coating. This printing capability evaluation will continue in 2017, including printing runs of additional paste formulations as well as further analysis of measured deposit volumes from prior printing runs.

APD2B. Thin Die Flipchip Assembly

Working in tandem with the internal development of new pick and place capability for very thin die (down to ~30 μm thick), the APL will demonstrate thin die flip chip joining. Initial efforts will be with conventional flux dipped flipchip solder interconnects, perhaps using temperature capable flexible substrates such as polyimide. Of particular interest will be the interaction of the solder reflow process and the inherent tendency for very thin die to distort out of plane. The ability for unconstrained mass

reflow joining of thin die may be possible only for die of less than some limiting X-Y dimension that scales with the die thickness. That is, thinner die are more prone to warp out of plane and therefore can only be expected to maintain adequate bump contact for the joining for smaller die. Slightly thicker silicon will warp less and keep flipchip bumps within joining range of the mounting plane over a larger area. Beyond these limiting values of die size to die thickness ratio, joining with some physical hold-down scheme (like thermocompression bonding) may be required.

APD3B. Large Body BGA Characterization

Ever expanding I/O counts for high bandwidth applications drive very large body size substrates for the packaging of high performance processors and complex ASIC and FPGA die. Laminate substrate body sizes up to 55 mm are not uncommon in the enterprise server and network telecomm space. A common structure consists of a substrate with several buildup layers on a laminate core, a flip-chip attached die, and a metal heat spreader lid attached to the substrate with a perimeter adhesive and in thermal contact with the silicon device through a thermal interface material on the back of the die. The temperature induced warpage of this package structure is critically dependent of the properties of the materials selected for its construction. Given the large area footprint of such packages, the board assembly yield and interconnect reliability are in turn highly sensitive to that resulting warpage.

This project is a case study of large body BGA packages using representative materials as defined by interested member companies. Large body (55x55mm) flip-chip packages have been fabricated using thin core (600μm) laminates, large die (20mm) and coined copper lids. Warpage behavior will be characterized for a variety of die sizes, including at least one multi-die configuration. A comparison will be made between the responses of two different thermal interface materials (putty or grease formulations). The BGA interconnect thermal cycle reliability will be measured as assembled to an appropriately thick (0.125”) circuit board.

APD11A. Laser Selective Reflow for Flip Chip Assembly

Having access to an area Laser Selective Reflow tool in 2017 provides the APL with capability for hands-on trials of laser impingement chip assembly. The planned resident LSR tool has been previously demonstrated capable of Sn-Ag flipchip soldering with copper pillar interconnect at typical silicon die thicknesses (cf. REL12B). This project will alternately include an exploration of the advantages of LSR flipchip processing for very thin die assembly, as well as other flipchip process parameter investigations. Lower temperature joining methods for less temperature capable substrates will also be explored. Transient liquid phase bonding for instance would be interest.

APD11B. Thermal Characterization of Laser Selective Reflow for SMT Assembly

Area laser selective reflow (aLSR) has been demonstrated for flip chip solder attachment. In this case a near uniform area beam impinging of the back of a silicon die produces a relatively uniform heat under

the die to reflow the interconnect bumps. For the case of laser reflow for board level surface mount assembly aLSR is expected to produce local reflow conditions at each component unique to the physical attributes of the component (thermal mass, thickness, area, and emissivity). This project will instrument common component package types for careful temperature measurements during aLSR reflow. Peak temperature attained by the component body at solder reflow will be of interest, particularly for components known to be temperature sensitive.

Consortium Deliverables

The charter of the AREA Consortium is to perform member company inspired research and convey the body of knowledge acquired directly to the Principals in a practical and useful manner. This is done by providing information in various formats and means of transfer including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager and staff will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings, with audio commentary, will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Project needs may require the AREA staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.