AREA Consortium

Dear Members,

We appreciate the effort so many of you made to attend the 2016 Fall meeting held at the end of the month. Our membership was well represented and the level of participation appreciated.

The meeting agenda included discussion of some next generation technology that we're considering for future consortium research. Prominent among these was laser selective soldering. We've begun to explore this nascent technology for flipchip joining and shared some initial observations on the solder joint microstructures and package warpage behavior resulting from this rapid and localized reflow process. Also of interest to our laboratory are the challenges posed by very thin die assembly. Industry work in this area is being actively sponsored by Department of Defense through the NextFlex program. The technical objectives of this federal technology initiative were described by the program leader, Dr. Eric Forsythe, from the US Army Research Laboratory.

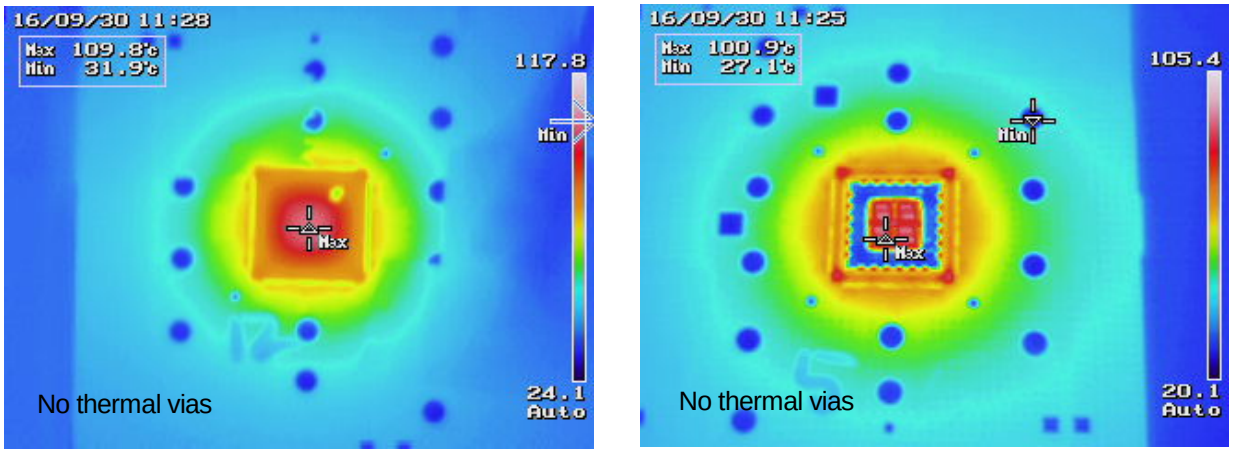
Sincerely,

Jim Wilcox
Consortium Manager

REL15B. Power Cycling of QFN Devices

Quad-Flatpack No-lead (QFN) packages are increasingly popular for power control devices. Such devices generate high power levels and consequently produce substantial local temperature gradients in and around the attached package. QFN interconnect reliability as determined through common laboratory environmental thermal cycle testing may therefore not be representative of such a locally powered device. This project uses the custom APL constant current source system to measure QFN solder joint reliability with a locally powered device.

A detailed thermal characterization of the QFN test devices was performed before proceeding with power cycle reliability testing. The thermal response of the assembled QFN was measured at various constant current loadings using an IR camera and the thermal diodes built into the test die. All heaters on the 5 x 5 mm test die were powered to produce a uniform die heading. The resulting thermal gradients visible from the top of the assembled package are shown in the left image below. Removing the plastic lid from the top of the package reveals the locally heated test die in the center of the package in the right image. Thermal performance was compared for QFNs assembled to test boards with and without thermal vias under the soldered central thermal pad.



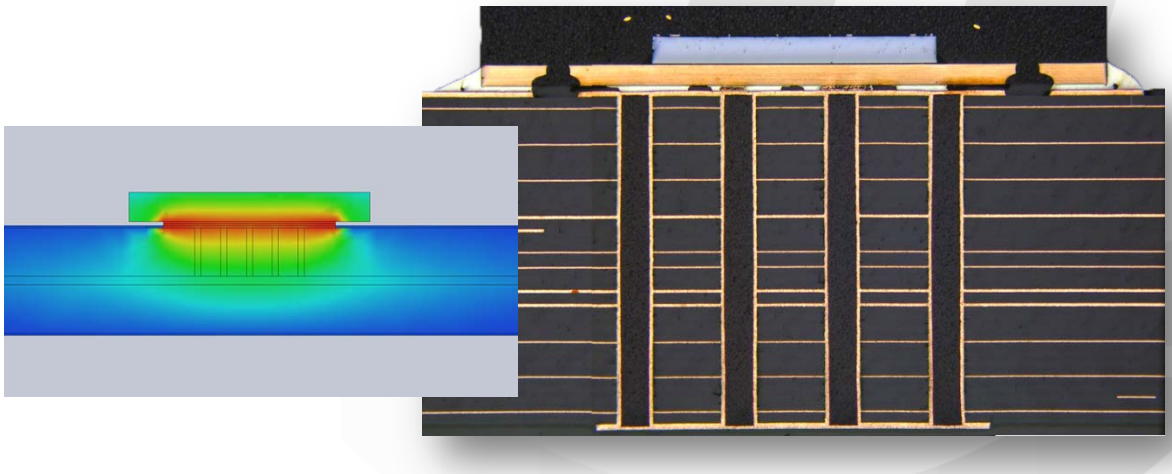
Infrared thermal image of powered QFN test package (LEFT) assembled to a test board designed without thermal vias. With the QFN plastic cap removed (RIGHT), the thermal image of the heated die is visible.

AREA Consortium

QFN Thermal Calculator

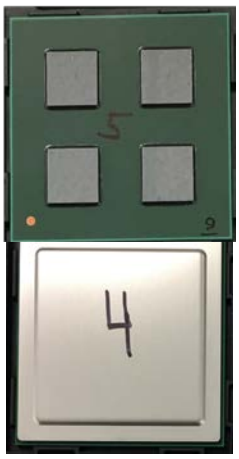
High power devices are commonly packaged in the simple, low cost QFN package. Adequate removal of the generous heat output of these devices is known to be critical for component reliability. This has led to persistent industry questions regarding the tolerable level of voiding in the soldered thermal pads under these devices. This question was addressed directly by one of our key consortium member companies through numerical simulation. Their Finite Element Analysis reveals that the overall heat transport out of a QFN power device is quite insensitive to voiding in the solder attaching the central belly pad of the device. That heat flux is however critically dependent on the number of thermal vias connected to the circuit board.

For ease of use, a simplified algorithm for this thermal analysis has been coded into a spreadsheet based calculator. It considers PCB attributes, thermal via design choices, and solder voiding level, returning the composite thermal resistance of the conductive path into the board. It is available for member download: QFN Thermal Calculator.



Right: Cross-section of typical soldered QFN structure. Voids are visible in the solder under the belly pad intended to transmit heat into the board through the four thermal vias visible in this section. Left: Graphic depiction of the thermal dissipation into the board as determined using FEA modeling.

APD3B. Large Body BGA Characterization



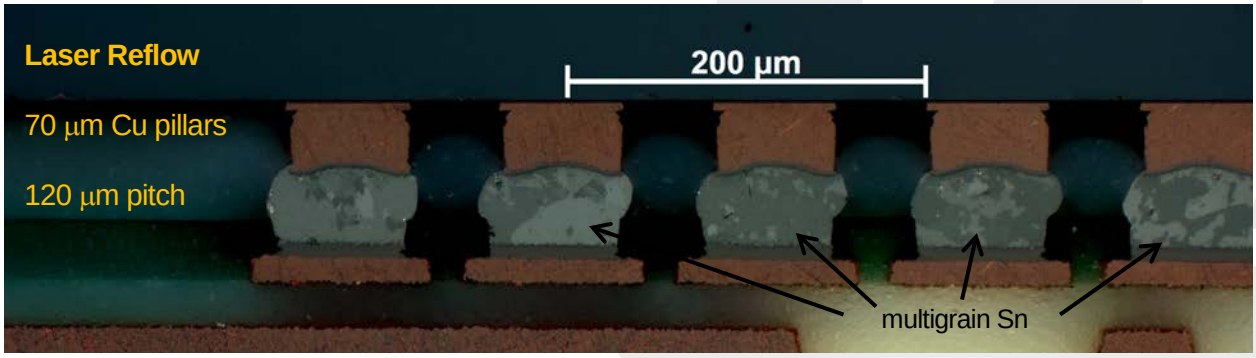
Large body (55x55 mm) flipchip PBGA packages have been fabricated for characterization of temperature induced warpage behavior and BGA reliability studies. Most samples were assembled with a single, large (20x20 mm) and thick (0.78 mm) silicon die characteristic of server processor or complex ASIC packages. One experimental cell with four-up, multi-die packages was also included for comparison. Lid attach was performed in the manufacturing line of a member company using coined copper lids. Two different thermal interface materials are included in the build, a Lord Gelease silicone gel material (MG-121) and a Shin-Etsu silicone elastomer (KJR-9086-2), to explore the TIM2 contribution to warpage and BGA interconnect reliability.

AREA Consortium

Laser Selective Reflow for Flipchip Assembly

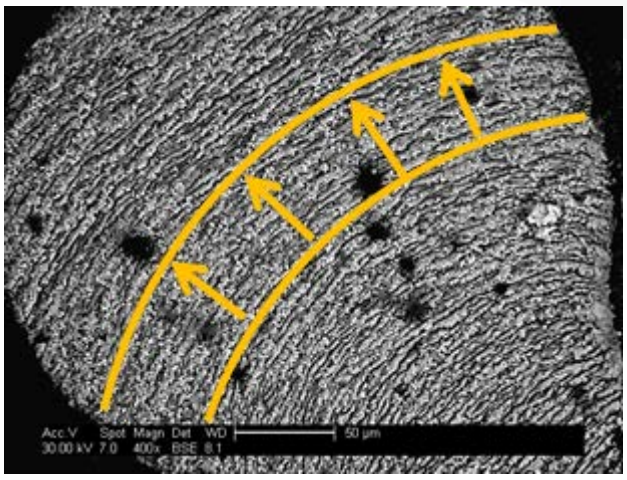
We've had some early looks at the Laser Selective Reflow (LSR) process for large die flipchip assembly. 20 x 20 mm test die were joined to large body laminate substrates using a defocused IR laser to provide a brief but controlled selective area solder reflow. The resulting flipchip joints were compared directly to those of companion parts attached with a conventional forced convection mass reflow process. The duration of the LSR profile was approximately eight seconds compared to 240 seconds for the convection mass reflow process.

Given the brief melt time of the laser reflow process (~3 sec), solder bump wetting was found more likely to stay localized on the tips of the copper pillars, rarely breaching the boundaries of the Ni barrier layer cap to wet the sides of the pillars. In the mass reflow equivalent, solder bumps were more likely to produce some wetting along the sides of the pillars. In those instances when mass reflowed bumps did stay localized on the Ni barrier layer, joints invariably solidified as Sn single crystal solder joints. In the more rapidly solidified LSR joints, multigrain Sn structures would result.



Cross-polarizer image of the outer row of copper pillar flipchip joints formed with Laser Selective Reflow.

REL16A. Die Size Effects on BGA Reliability – Thermal Fatigue Fractography



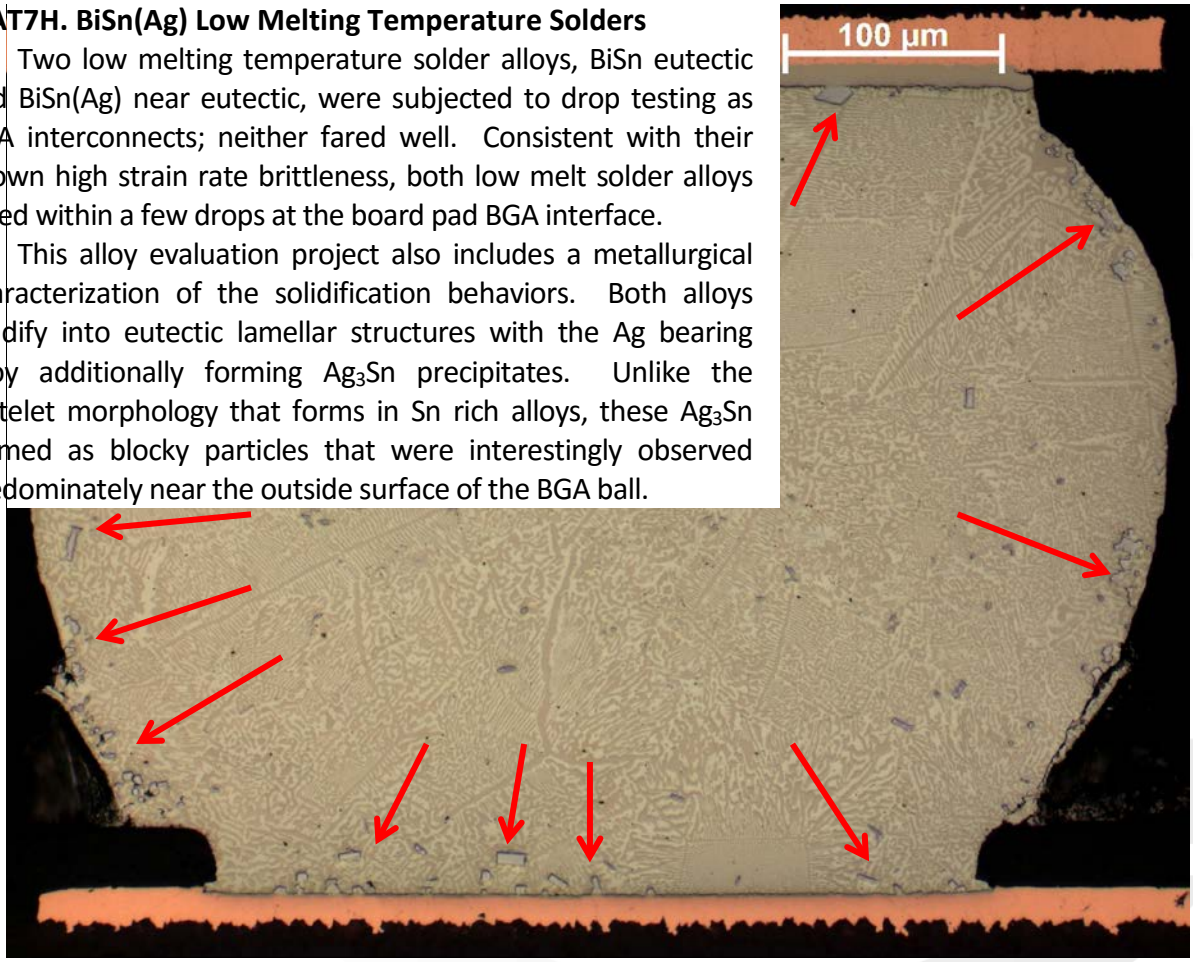
Fatigue striations visible on the board pad after extensive thermal cycling indicate the incremental progression of a fatigue crack along the base of the BGA joint [-40/125C cycle].

Our study of Die Size effects on package interconnect reliability continues. Testing of the longer lived parts in the 0 to 100C thermal cycle is nearing completion. Failure surfaces have been mechanically exposed to permit fractographic examination of individual failed connections. On some joints (not all) clear fatigue striations are visible on the fracture surface indicating the crack growth increment for individual thermal cycles. While this classic fatigue mechanism is clearly operative in some solder joints, it may not be the life limiting failure mode for much of this sample population. An alternate failure mode, which ultimately determines the thermal cycle reliability for the three die size packages, appears to be operative at the package corners. These early corner failures produce an inverse square dependency of the package thermal cycle lifetime on the die DNP for the die sizes tested.

MAT7H. BiSn(Ag) Low Melting Temperature Solders

Two low melting temperature solder alloys, BiSn eutectic and BiSn(Ag) near eutectic, were subjected to drop testing as BGA interconnects; neither fared well. Consistent with their known high strain rate brittleness, both low melt solder alloys failed within a few drops at the board pad BGA interface.

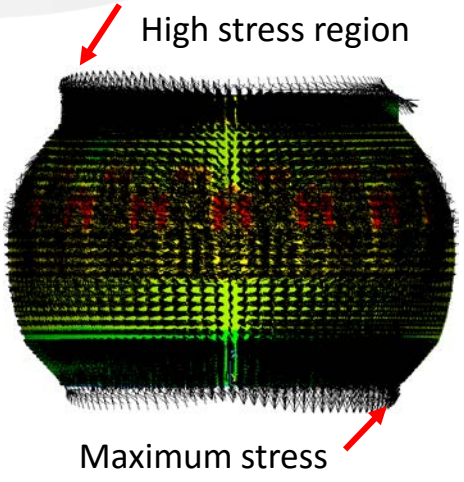
This alloy evaluation project also includes a metallurgical characterization of the solidification behaviors. Both alloys solidify into eutectic lamellar structures with the Ag bearing alloy additionally forming Ag_3Sn precipitates. Unlike the platelet morphology that forms in Sn rich alloys, these Ag_3Sn formed as blocky particles that were interestingly observed predominately near the outside surface of the BGA ball.



REL3D. Elevated Temperature Harmonic Vibration

A finite element model has been created to describe solder joint loading in the BGA256 component during harmonic vibration at elevated temperature. The model evaluated the stresses imposed on SAC305 solder joints by the deflection of the test board during vibration loading (assuming high temperature PCB materials properties). It further simulated the solder joint stresses imposed by thermal mismatch at high temperature (assuming initially stress free solder joints at room temperature).

Combining these stresses through superposition identified maximum solder joint stresses during high temperature harmonic vibration. The location matched well with the observed failure locations. Vibration testing at 120C produced solder joint failures at the board side interface, unlike room temperature vibration which was prone to solder failures near the package side interface.



Vector plot of maximum principal stresses at 120C in a corner solder joint at peak board deflection (downward).