AREA Consortium

advanced process lab
research • process support • analysis

Dear Members,

I have just returned from meeting #27 of the IPC PERM* Council. While our military and aerospace brethren there continue to express longstanding concerns about uncertainties in the harsh environment reliability of Pb-free electronic assemblies, several did acknowledge the growing body of Pb-free commercial products with reliable field performance. A major work item for the council has been the compilation of design guidelines for Pb-free military electronic products that capture the industry learning from the last decade of Pb-free commercial products.

I shared with them a broad overview of the analytical methods, metallurgical characterizations and reliability testing techniques that could and should be used for evaluating new Pb-free solder alloys. AREA consortium members have long been getting the benefit of this full array of evaluation methods used by our staff and students to understand the latest electronic solder materials. Results from these solder evaluation methods are regularly on display at our face to face project status reviews.

Speaking of which, it's time to start making travel plans for our next consortium meeting. We've booked it for March 30-31, 2016 at the usual venue on the Binghamton University research campus. The agenda will include our usual full scope of assembly/materials/reliability topics. We will be broadcasting the final agenda shortly. Please plan to join us.

Sincerely,

Jim Wilcox
Consortium Manager

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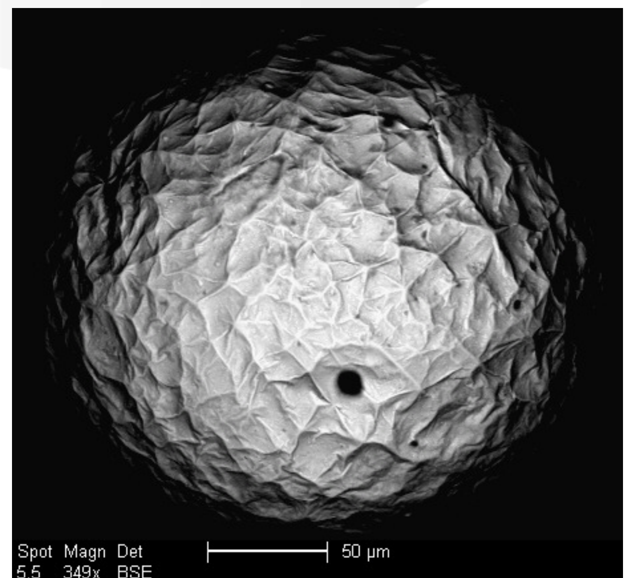
*PERM = **P**b-free **E**lectronics **R**isk **M**itigation

MAT7E. Alternate Lead-free Solder Alloys

Initial (as-assembled) microstructure characterization for the alternative solder alloy study is nearing completion. The analysis includes detailed characterization of secondary phase precipitates as well as the baseline Sn grain morphology for each of the component types. Recall that this extensive experiment evaluates the thermal cycle reliability of Innolot, Violet, and two other experimental SnAgCu based alloys micro-alloyed with Bi and Sb. ENIG and Cu-OSP finish boards have been included.

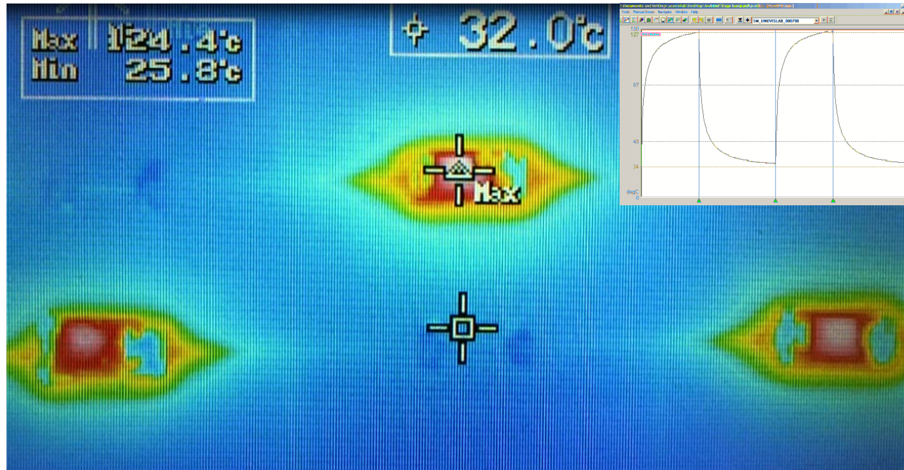
Solder joint failures are starting to accrue for the least reliable components in the most severe thermal cycle (-40/125C). No failures have yet been reported with the milder 0/100C profile. Test boards allocated for the mildest cycle (20/80C) have been assembled and wired for test but are still awaiting available ATC chamber space.



Solidification texture of a 10 mil sphere of the high temperature automotive solder alloy, as attached to the CVLGA360 component, prior to SMT assembly.

REL15B. Power Cycle Reliability Test Method

The electric current required to produce various steady state peak temperatures is being calibrated on the Power Cycle test board. 20 ohm 1206 resistors and 100 ohm 0805 resistors are being used for this exercise. The constant current supplies now being built for the power cycling test have been designed for running at various fixed current levels. Planned cyclic reliability tests will apply current with a square waveform to achieve predetermined peak component temperatures. Alternating resistor sites are populated for this calibration exercise to better isolate the heat formation from individual devices. Some heat can be seen to dissipate along the copper traces to the right and to the left of each device. The circuit board remains at the ambient temperature.



Inset: heating and cooling rates for current applied with a two minute period square wave.

Infrared image of 1206 capacitors achieving a peak temperature of 124C with 150mA current.

REL6A. Solder Print Correlations to Reliability

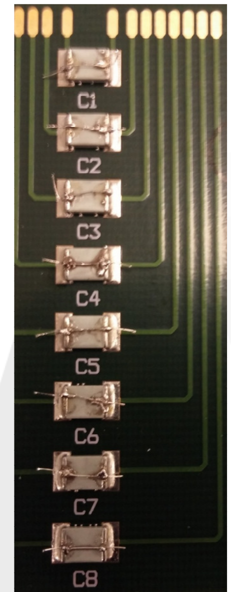
Our first large scale study comparing the effects of solder paste deposit outliers to assembly yield and component reliability has recently concluded. By intentionally producing undersized paste deposits at select solder joint positions for BGA, LGA and QFN components we have found that there can be significant consequences to both yield and reliability. Not surprisingly, our findings indicate that the different devices have unique sensitivity to the outlier paste deposit volumes.

Firstly, we have found that a low volume outlier deposit, when occurring at the selected solder joint positions, typically *reduces* the thermal cycle lifetime of Bottom Terminated Components (LGA and QFN). Additionally, by analyzing the paste deposit volume for every solder joint that led to LGA and QFN component failure, we can show that as the outlier volume decreases, the characteristic lifetime decreases. Secondly, the results for the BGA devices indicate that reducing the paste deposit volume at select solder joint positions can *improve* component lifetime. This confirms results previously reported by the AREA Consortium. At this time it is theorized that the reduction in paste volume results in a slightly more compliant BGA solder joint.

REL16A. Die Size Effects on the Reliability of BGA Package Interconnect

The effect of silicon die size on BGA component reliability is being measured in support of a reliability modeling exercise. Otherwise identical molded BGA packages were obtained with three different die sizes. Although increasing die size is fully expected to decrease package lifetime, the extent of the decrease is not readily predictable. The unassembled warpage characteristics of the devices have been evaluated using Therm-Moire™ and assembled specimens are now in -40 to 125C thermal cycling. Nearly 1000 cycles have been completed with most of the large die samples already having failed. Additional samples are being prepped for strain and CTE analysis which we hope to have completed shortly.

MAT6D. Component Terminations for Elevated Temperature Operation

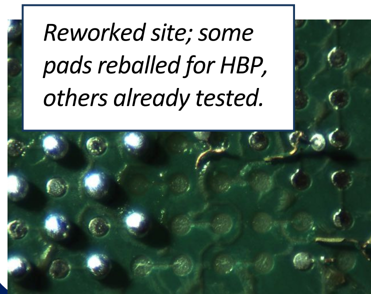


Detailed microstructural characterization of the solder joints attaching elevated temperature rated capacitors (Presidio) has been completed. These results will be reported at the upcoming consortium meeting in March. The project review will include observed metallurgical reactions with the various experimental surface termination finish and solder alloy combinations under evaluation. Consistent with the intended application space of these devices, the robustness of these solder connections will be tested through extreme temperatures. All assemblies are being subjected to a -50 to 200C thermal shock test. In order to use in-situ event detection for monitoring the integrity of these joints, a fine jumper wire has been soldered across the top surface of each capacitor (see photo). Jumper attachment solders were of compositions matched to that of the solder fillet on test. Only a minimal connection on the top surface is allowed to avoid disruption of the tested joint in the fillet. The baseline capacitance of each device has been recorded prior to this modification and will be reconfirmed after the repeated thermal shock exposure.

MAT1B. Reworkable Component Underfills

All the TB2015U boards have been assembled using Sn/Pb eutectic solder with a portion being sent to the KYZEN corporate technical center for controlled cleaning prior to underfill. New underfill materials have been procured and programming of the ASYMTEK dispense tool is complete. Underfilling will commence as soon as the cleaned boards are returned.

Thermal cycling of the prior TB2014U boards continues. The second group of underfills (G and H) has exceeded 2000 cycles but some parts still have too few failures for good statistics. The first and (when available) the last failures have been cross-sectioned for failure analysis.

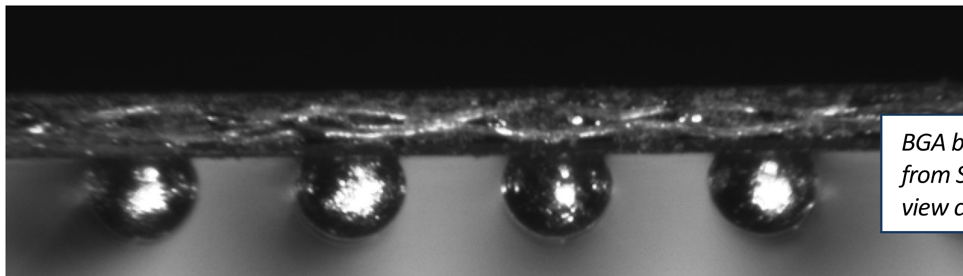


Reworked site; some pads reballed for HBP, others already tested.

Reworkability evaluations have also begun. Several underfilled components have been successfully removed and site cleaning methods attempted. Recommendations from the underfill suppliers have been sought regarding the optimum site cleaning process to minimize pad and mask damage. Hot bump pull (HBP) pad strength tests have begun on samples at all planned stages to characterize the PCB damage incurred from the rework process.

APD9A. Warpage Contribution to Head on Pillow Defects

A side view camera has been installed on the Scorpion rework tool to allow video capture of BGA ball wetting events during the SMT solder attach process. To provide some objective measure of the magnitude of substrate warpage likely to produce HoP defects, the wetting of BGA balls by solder paste deposits will be observed at fixed elevations above the board pads.



BGA ball image from Scorpion side view camera.

MAT8B. Conformal Coating Studies

The -40 to 125C thermal cycle test phase for the UV50LV, UV40 and Semblant Plasmashield 400 coating materials is complete. Nearly 3000 cycles were accumulated on the coated and non-coated baseline boards. Data analysis and failure analyses are in progress. Early results indicate that all three conformal coatings compromise the thermal cycle performance of at least one device type evaluated (resistors, BGAs, QFNs, LGAs), but overall the results for the Plasmashield 400 are very encouraging. We also continue to test these same materials in a -20 to 80C thermal shock cycle. This cycle is far milder than the -40 to 125C test and we expect samples to survive 3 to 4 times as many cycles in this environment. This test was included in the experiment because conformal coatings such as UV40 have relatively low Tg and are not marketed for high temperature environments such as that simulated by the -40 to 125C thermal cycle.

An additional study comparing the effects of Parylene C and Plasmashield 400 when applied to surface mount resistors is also underway. The Plasmashield 400 material on these test boards appears to be degrading quickly in the -40 to 125C thermal cycle. This effect may be due to excessive handling of the samples by foreign customs officials prior to the coating application. Testing of Parylene C continues nonetheless and we have completed approximately 1000 cycles to date.

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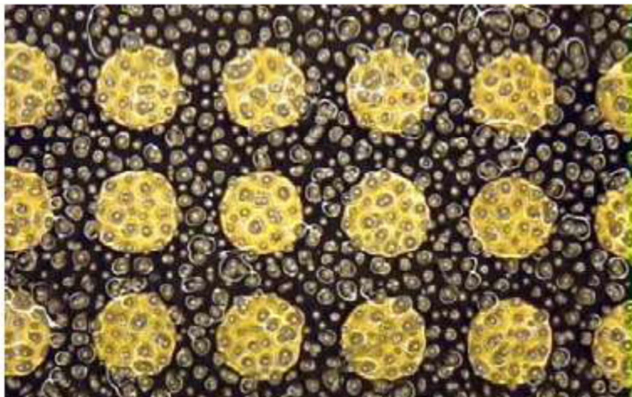
MAT9A. Conductive Filled Elastomer Connections

Some highly temperature sensitive components such as optical transceivers may not be able to tolerate the processing temperatures required for Pb-free solder assembly. One alternate connection method considered for such devices is Anisotropic Conductive Films. These connections can be made at room temperature through a compression socket. One such ACF material is the PariPoser®, a silicone elastomeric film containing distributed electrically conductive spheres.

We have begun characterizing the reliability performance of PariPoser conductive film in high temperature, high humidity (85C/85%RH), and -40 to 125C thermal shock environments. The PariPoser is supplied in a socket housing attached to the motherboard through a metal backer plate. A compressive load is applied to the component through the use of a leaf spring that locks onto the housing. This load compresses the underlying ACF producing localized electrical conductivity from the component of interest to the circuit board connection pads. In our experiment PariPoser film has been used to connect a dummy LGA style component. This LGA was acquired at three different thicknesses in order to evaluate the PariPoser interconnection conductivity and insulation resistance at three distinct compressive loads.



Printed circuit board contact pads viewed through the PariPoser anisotropic conductive film. Ag plated Ni spheres are visible.

Thus far we have characterized the electrical performance of the PariPoser assembly by using a data logger to record resistance changes during the humidity and thermal shock tests. Initial results indicate that the lowest compressive load evaluated resulted in electrical failures at lower temperatures than the higher compressive loads, although all three load levels occasionally resulted in an electrical failure above 115C. The exact reason for electrical failure is not yet understood, although thermal expansion and warpage are likely factors.