advanced process lab
research • process support • analysis

AREA Consortium

Dear Members,

We will soon be embarking on a new packaging assembly initiative. The equipment engineering team here at Universal Instruments will be developing and implementing capability for thin* die handling in our placement tools in the coming year. This new tool capability provides us a great opportunity to fold a corresponding thin die assembly process investigation into our consortium research portfolio. Knowing that standard thickness silicon die on laminate substrates drives temperature induced warpage and a variety of consequential assembly defects, we're expecting some assembly manufacturing benefits from using extremely thin die. These could include reductions in the occurrence of 'white bump' die defects, head-on-pillow BGA defects, and laminate pad cratering on SMT reflow cooldown—all benefits over and above the prime project motivation of enabling manufacturing enhancements for 3D packaging integration and further reductions in package volume for consumer and mobile products.

We're planning to discuss this initiative in some detail at our next consortium meeting on October 26th. Please make plans to join our discussion at this meeting. We'd love to incorporate your insights in our program planning.

*(30 – 75μm thick)

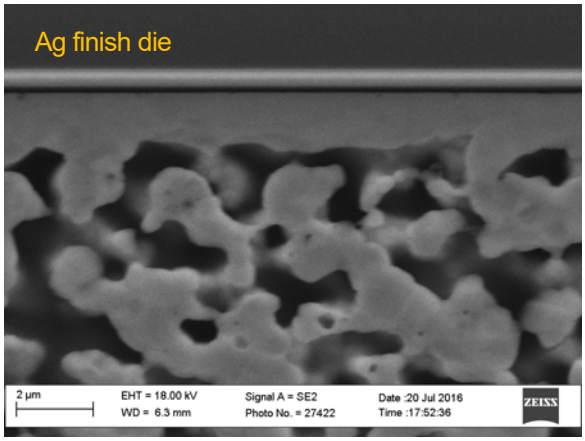
Sincerely,

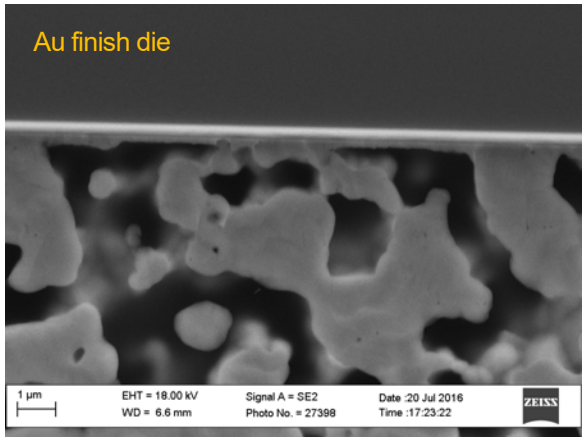
Jim Wilcox
Consortium Manager

MAT6B. Sintered Silver Die Attach

Sintering experiments at different times, temperatures and atmospheres are on-going. These are targeted at understanding the impact on die shear strength for either Ag finish or Au finish die. Of particular interest is the development of silver structure at the bonded interface. Invariably, this local interfacial structure has determined the mechanical integrity of the attachment. Photos below illustrate the dramatically different interfacial structures formed on Ag and Au finish die.

Aging experiments are used to confirm the long term stability of these as-sintered structures. Short term thermal aging samples have now been analyzed. Longer term aging is still in progress with samples which will be removed from high-temperature storage in mid-September.



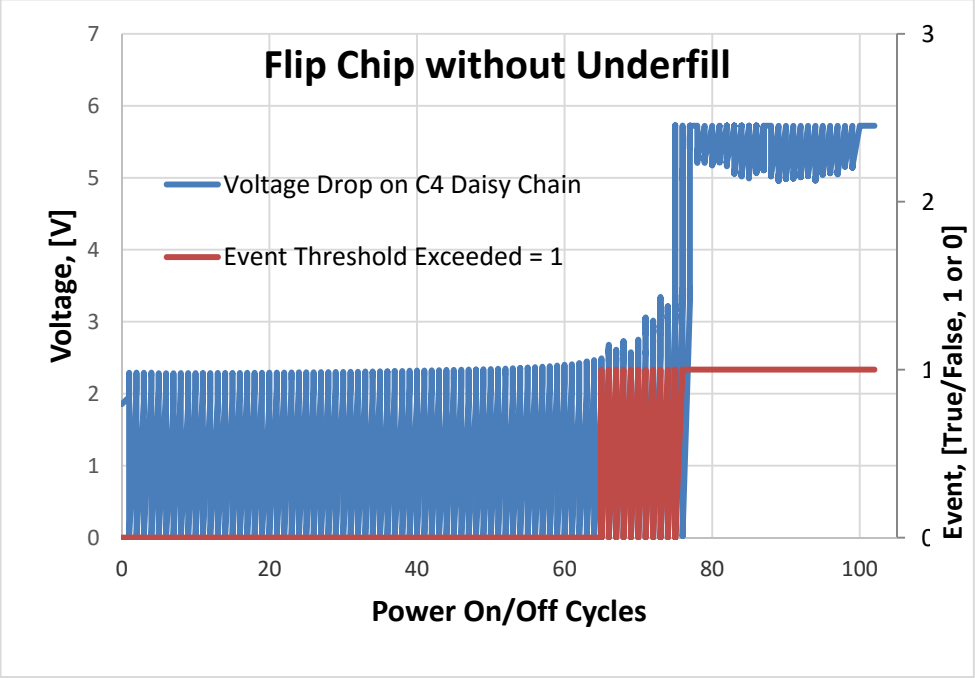


Sintering of silver paste against a silver finish die (LEFT) produces a robust layer of dense silver at the interface. This dense layer is absent on the gold finish die (RIGHT) despite an identical sintering schedule.

REL15A. Power Cycle Reliability Test Method

Component level power cycle testing capability has been developed and now implemented in the APL. A computer controlled constant current circuit (CCC) has been designed, prototyped and fabricated. Up to 64 test channels are available per CCC unit, each producing individually defined constant current through the selection of an appropriately sized pluggable resistor. By systematically changing the pluggable resistor, the current that is required to resistively heat the device-under-test (DUT) to a target temperature, for example 125°C, is identified. The CCC includes embedded event detection capability with a threshold voltage drop that is entered in a front panel user interface. Also, a digital multimeter under program control measures the voltage drop across nets of daisy chained solder joints. Visual Studio 2013 was used to write the C# code and user interface for setting up and controlling a power cycle test.

Two verification trials have been conducted to demonstrate the power cycle test capability. Discrete resistors, 16 each of sizes 0805 and 1206, have been cycled with a constant current square wave to produce an ambient to 125C temperature cycle in the device body. A first group of eight resistors of each size ran through 3112 cycles without any fails and the second group of eight reached 2181 cycles without any failures. The CCC unit performed flawlessly and the data collection algorithm proved stable. To confirm the failure detection circuitry, a flip chip without any underfill was tested using a power cycle to 125°C. Consistent with our expectations from prior thermal cycle experience, failure was detected at 65 power cycles. Digital events that exceeded a 10% increase in voltage drop (resistance increase) were first detected during the power-on segment of cycle 65 (see plot below). During the subsequent power-off segment of the cycle, the event signal cleared. On cycle 66, the analog voltage drop on the flipchip daisy chain was measured to exceed the 2.52V threshold (*i.e.,* >10% increase in resistance.) During the power-on portion of cycle 75, event detection indicated sustained voltage drop that exceeded the threshold. Similarly, during cycle 75, analog voltage drop measurements indicated a fully open daisy chain net. During the power off portion of the cycle, only a small detection current is flowing (<0.5 mA) and therefore the measured voltage drop is near zero.

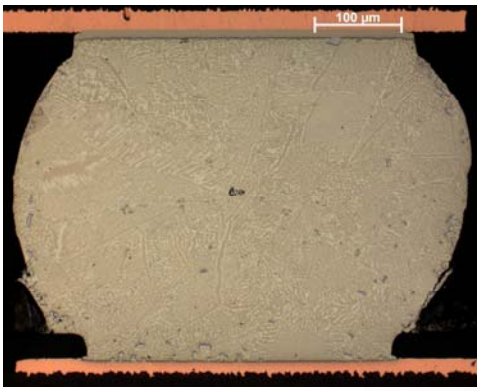


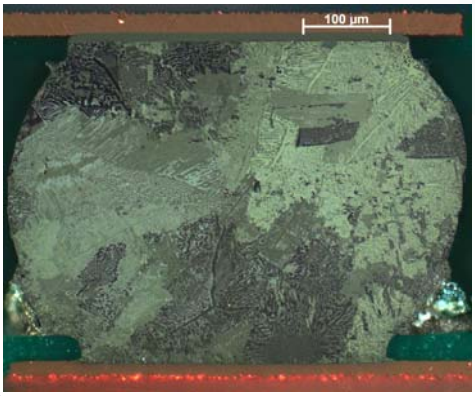
Output of tandem failure detection circuits in the power cycle system for a flipchip solder joint circuit. Analog test net voltage drop (blue) corresponds well with digital event detection signal (red).

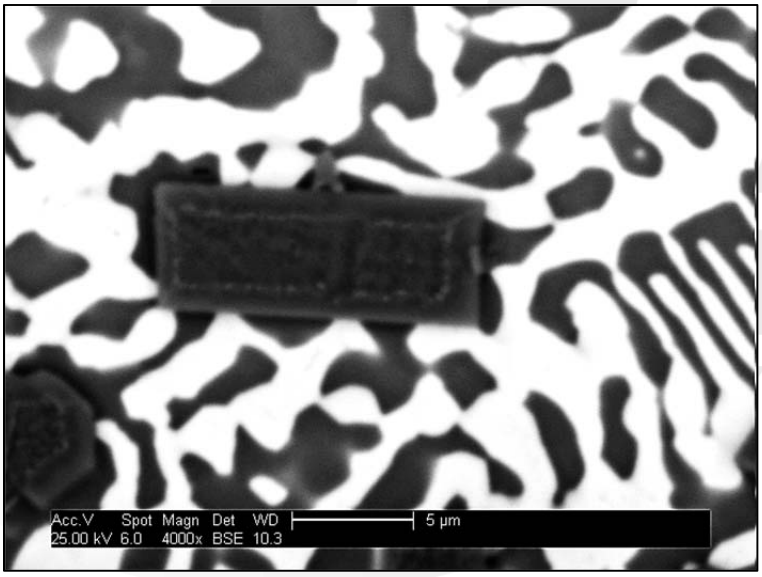
MAT7H. SnBi(Ag) Low Melting Temperature Solders

Typical Pb-free solder processing temperatures are known to damage various temperature sensitive passive devices such as electrolytic capacitors and LEDs. Perhaps more significantly though, these high reflow temperatures exacerbate warpage induced soldering defects on large body BGA packages including head-on-pillow defects, BGA non-wets, and PCB laminate pad cratering from high cooldown stresses. Low melting point solder alloys may alleviate many of these challenges.

Our low melt solder evaluation program has begun with two alloys: eutectic 58Sn42Bi and 57Sn42Bi1Ag. These alloys melt ~140°C compared to the 217°C melting point of standard SnAgCu eutectic. Our study of these alloys covers solidification behavior, surface finish effects, microstructural analysis, and mechanical testing (shear strength, hardness, vibration) at room temperature and elevated temperatures as well as ambient drop shock testing. Measurements of shear strength in as-reflowed single sided solder joints are complete for two surface finishes. Solder joints produced with two different reflow TAL times and aged up to 10 days at 125°C have been tested. All additional samples required for other planned mechanical tests have been fabricated.







(a) Bright field image of 57Sn42Bi1Ag solder joint on Cu-OSP board finish and 60s TAL reflow. (b) Cross polarized image of the same joint, and (c) an SEM image of the eutectic lamellae with a Sn rich (dark) phase and Bi rich (light) phase. Blocky third phase particles are seen throughout.

MAT7E. Alternate Pb-free Solder Alloys

Our comprehensive evaluation of several third generation Pb-free solder alloys continues to accrue reliability data from three different environmental thermal cycle profiles. A significant number of failures among the TB2015 component set on test have now been reported for the 0/100°C profile. The milder, longer term 20/80°C profile test has begun to see failures as well, primarily in the LGA256 component for two candidate alloys.

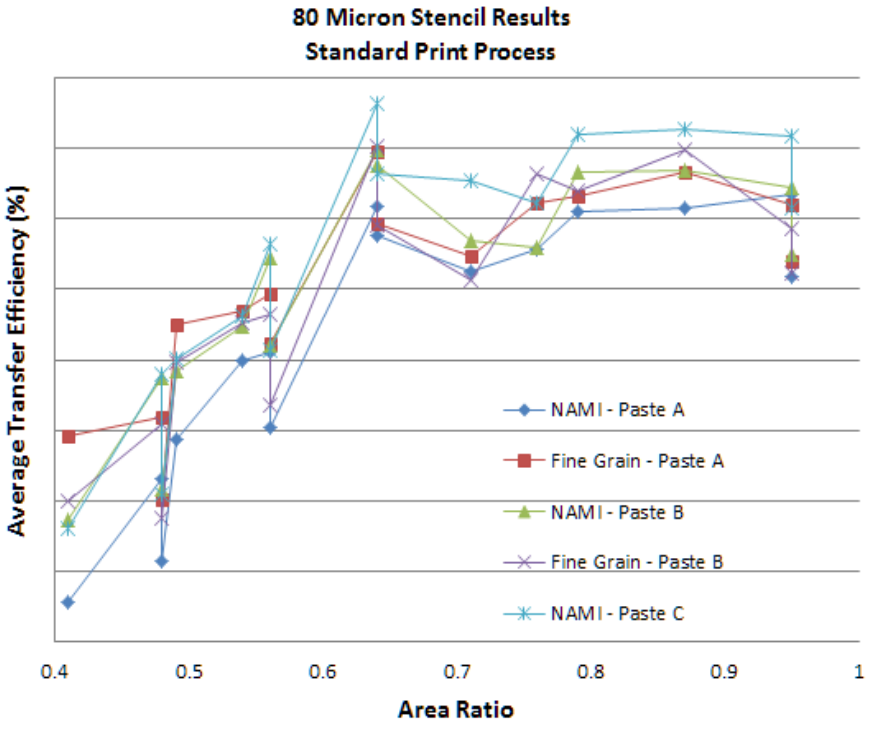
Analysis of failures from the harsher -40/125°C cycle is complete for several components: LGA256, LGA208 and BGA208 on both Cu-OSP and ENIG surface finishes. Characteristic failure modes are being tabulated for each alloy:finish combination. These include bulk solder failures, laminate pad cratering (with trace failures), intermetallic failure or interfacial separation.

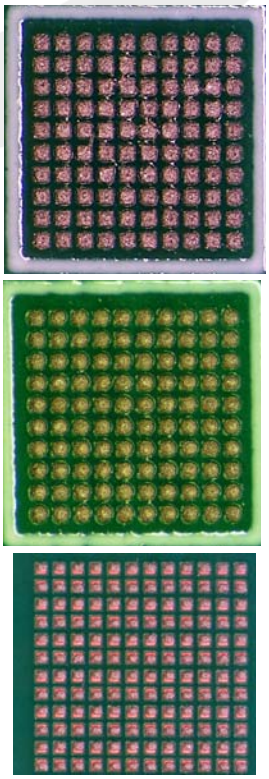
Effect of Reflow Oven Static Pressure on Solder Joint Void Formation

A new project has been defined to evaluate the effect (if any) that reflow oven static pressure has on the formation of solder process voids during SMT reflow. The ability to adjust static pressure in the reflow environment exists in our new BTU Pyramax 125N oven. We are currently developing two similar reflow temperature profiles for a lead-free assembly process with either a high (1.1 in-H_2O) or low (0.5 in-H_2O) static pressure. The solder joint quality (void level) of Land Grid Array (LGA) and Quad-Flat No-lead (QFN) solder connections produced with these profiles will be compared directly. Test boards and components, including three QFN and three LGA component designs along with several CSP and BGA devices have been set aside for the project. Two solder pastes have been acquired for this study: one characterized as a "low-void" formulation and a second with "moderate" void formation properties, the latter intended as the benchmark material.

Fine Pitch Printing

The first 16 legs of our Fine Pitch Printing 2016 project are now complete. Thus far we have compared print characteristics of 50 and 80 micron thick stencils with NAMI nanocoating and an 80 micron thick stencil fabricated with fine grain steel. These comparisons were done using three different solder pastes with both standard printing and ProActiv (vibratory) printing. Early results indicate that the fine grain and nanocoated stencils produces comparable transfer efficiencies for area ratios in excess of 0.64 while significant variability was observed for lower area ratios.





Left: Sample results from KohYoung SPI tool illustrating transfer efficiency for various stencil types. Right: Visual images of paste deposits are also being captured to reveal qualitative print differences.