ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2016 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium executes manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and assembly process for AREA Principals. Research ranges from scientific investigations on fundamental materials behavior to topics directly applicable to manufacturing challenges. In each case, the objective is to provide AREA Principals with meaningful data that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals often encounter resource constraints that limit internal research activities critical to product needs. They are therefore encouraged to view the consortium research staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a comprehensive website with on-demand content is made available (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals and the AREA Steering Committee. The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities as needed.

The primary focus for 2016 will be the initiation and/or the completion of the projects outlined in this document. Additional topics may be added throughout the year as materials are provided and interests develop, given the availability of resources. The 2016 research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

Materials

Advances in assembly materials often provide manufacturers with the means to improve process yield or product reliability. The breadth of available materials and opportunities for complex materials interactions can however result in significant implementation challenges for emerging technologies. AREA Principals are faced with evaluating the properties of these materials, identifying the assembly process window and measuring material performance through accelerated qualification tests. A key mission of the AREA Consortium is to provide its Principals relevant and timely information in these arenas to alleviate such new materials challenge. The Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact of their use.

MAT1B. Reworkable Component Underfills

Evaluation of the dispense process and reliability performance of various board level capillary underfill materials will continue in 2016. On-going work is focusing on those materials marketed as thermally reworkable formulations. Materials being evaluated include reworkable offerings from Zymet, Namics, Henkel and HB Fuller. While the process work was completed in 2015, reliability tests (for SAC305 interconnect) and rework evaluations will continue through 2016. A select subset of boards will be allocated for alternate profile thermal cycle (*e.g.*, -20 to 80°C). Additionally, select underfill materials will also be evaluated on TB2015U test boards assembled with SnPb eutectic solder. Consistent with Mil/Aerospace industry practice, these latest boards will be sent through a post assembly wash operation prior to underfill. Thermal cycle reliability of the TB2015U component set in the as-underfilled state (non-reworked) will be tested for each of these materials. The rework capability of these materials will be explicitly explored. The process of underfilled component removal and site redress will be exercised prior to examination for damage to the PCB mounting surface.

MAT4B. Thermal Characterization of Putty Thermal Interface Materials

The need to remove ever increasing amounts of heat from high performance semiconductor packages is becoming more of a challenge using standard TIMs. In addition, degradation of thermal conductance in the field is a significant risk for high power electronics expected to remain in service twenty years or more. This research evaluates the performance of several thermal putty and/or thermal grease materials from various suppliers using the component level TIM tester developed in 2012. The project is divided into two parts: process development and thermal characterization. A deposition process will be developed for each material using an Asymtek™ dispenser. The thermal behavior of each will be characterized at time zero for a fixed bondline thickness and again after high temperature storage. Time permitting, assembles will be thermally cycled to evaluate the “pump out” risk for these lightly cross-linked materials.

MAT6: Harsh Environment Electronic Interconnect Research

As electronics become integrated into higher temperature environments such as those associated with deep well drilling and distributed controls in the automotive and aviation applications, higher melting temperature solder alternatives are needed. In 2016 the harsh environment electronics thrust will continue to focus on the materials, assembly, and reliability of high temperature electronics packaging. A high temperature polyimide test board has been designed and sourced for projects in this research thrust.

MAT6C. Sintered Silver Die Attach Materials

High temperature die attach materials are critical for the operation of next generation wide band gap semiconductor devices in power electronics applications. These products operate at substantially higher temperatures than conventional electronics. With currently available materials, a metal based die attach system is required to provide adequate thermal conductance to extract the waste heat. Previous AREA work evaluated candidate high temperature Pb-free solder alloys for this die attach application. This latest project will focus solely on various sintered silver die attach materials designed for pressure-less processing. The scope will include optimization of the thermal sintering process, detailed characterization of the microstructure, joint strength and thermal stability.

MAT6D. Evaluation of Component Terminations for Extended Elevated Temperature Operations

Surface finish effects have been well studied for active component package types such as BGA or LGA. Component surface finish effects on small passive devices however are relatively unknown. The surface area on a passive device termination relative to its associated solder joint volume is often quite large such that the finish could have outsized effects on the joint metallurgy and interconnect reliability. Use of these passives in high temperature applications may further exaggerate the metallurgical impact of surface finish.

This project studies how the surface finish of passive devices affects interfacial reactions, microstructure, and mechanical behavior of the board interconnects. The test device used is a 1712 size high temperature capacitor, making the results particularly applicable to high temperature electronics. These capacitors have been provided with various surface finishes (including Au, Ag, Pd-Ag, and matte Sn). High temperature reflow assembly processes have been defined for attaching them to a polyimide test board using BiAgX, Innolot, or Pb5Sn2.5Ag solder alloys. Ag-filled epoxy has also been included as another Pb-free alternative. Device shear tests (at ambient and 200°C) have been completed for various solder-finish combinations along with the associated fractography. High temperature storage and thermal shock (-50C to 200°C) evaluations of these joint combinations will continue through 2016. Metallographic analysis will link microstructural observations to observed mechanical behavior and fatigue performance.

MAT6F. Pb-free Solder Alloys for Engine Control Applications

Solders intended to withstand the high operation temperatures such as those encountered in automotive under-the-hood applications (~200˚C) have historically depended on high Pb alloy formulations. The ever expanding scope of global product environmental regulations has motivated a search for Pb-free solder alternatives for these applications and similar aviation engine control applications.

This project studies the microstructure evolution and thermo-mechanical reliability of three new Pb-free solder alloys in high temperature environments. Candidate solder alloys are Sn based with various alloying elements will first be screened through high temperature storage and shear tests at selected simulated maximum operating temperatures (150°C, 175°C, 200°C). A common high Pb alloy (Pb10Sb5Sn) and SAC305 solder are included as controls. The ambient and high temperature shear strength behavior will be analyzed in the context of microstructural evolution and interfacial intermetallic growth behavior. The thermo-mechanical reliability of promising candidate alloys will be studied through high temperature thermal shock tests. An assembly test vehicle has been sourced that includes various component types: BGAs, QFPs, and surface mount resistors, among others. Characteristic lifetimes and failure mechanisms will be compared to those of the control alloys. Microstructural analysis will be used to help interpret lifetime trends and observed failure modes.

MAT7: Lead-Free Solder Alloy Evaluations & Microstructure

Lead free solder alloys with various alloying elements and dopants are being evaluated by the industry as drop-in replacements to the standard SAC305. Suppliers claim that dopants in these alloys result in various property enhancements such as improved drop test performance. The reduced silver content often leads to lower material cost. Previous AREA results have shown that mechanical and thermal reliability improvements can be correlated to microstructural differences created by varying solder volume and PCB surface finish. Significant effects of solder volume and composition on microstructure and thermomechanical performance of various lead free solder joints was observed.

Projects included in this alternate solder alloy thrust include evaluations of microstructure and mechanical properties for various solder alloys on different pad finishes. The work encompasses characterizations for both individual solder balls as well as components assembled onto test boards for true second level reliability comparisons, either by ATC or mechanical testing. Another objective of this work is to quantify the performance of new lead free solder joints relative to common SAC 305 and SnPb alloys. Included in this work are SnPb controls and a mixed solder technology build consisting of lead-free solder joints and SnPb paste.

MAT7E. Surface Finish, Solder Volume and Mixed Alloy Effects on Thermal Cycle Reliability

The continued shrinking of components for ever denser handheld electronics brings new reliability questions. It is well known that the microstructure of lead-free solder alloys is significantly affected by solder joint volume and composition and that the microstructure in turn greatly affects the reliability of the solder interconnects. In this work we will analyze the effect of PCB surface finish on microstructure and reliability of BGA and LGA package interconnects in accelerated thermal cycle test. The effect of PCB surface finish (Cu-OSP and ENIG) and solder volume on Sn grain morphologies (beach ball, interlaced or single crystal) of various commercial components is investigated. The ATC performance of several new alloys (such as Innolot, Violet, and two other alloys microalloyed with Bi and Sb) will be compared to SAC305, SAC 105 and eutectic SnPb solder alloys. Careful microstructural analysis on as assembled samples and failed samples is planned. The thermal cycle failure mechanisms of both LGA and BGA packages will be compared across different cycling profiles (-40/125°C, 0/100°C and 20/80°C).

MAT7F. Thermal Cycle Reliability of Mixed Solder BGA Assemblies

The reliability performance of SAC solder joints with the addition of Pb is always regarded with skepticism. Discrepancies exist in the literature regarding the effect of Pb addition on microstructure and thermal cycling performance of SAC solder joints. This work examines the consequences of Pb incorporation into SAC305 BGA spheres during SMT reflow soldering. SAC305 BGA components will be assembled using a common SAC 305 reflow profile and SnPb eutectic solder paste. Both Cu/OSP and ENIG finish boards are used. Thermal cycle results of the mixed assemblies will be compared to others having homogenous SAC305 and SnPb solder joints. ATC testing will be performed at two different thermal cycling profiles (0 to 100°C and -40 to 125°C) to reveal fatigue acceleration factors for mixed assemblies. Microstructural analysis will A careful analysis will be performed to correlate the thermal cycling lifetimes to microstructure of solder joints.

MAT7G. Effect of Solder Alloy Composition and Test Parameters on Solder Joint Shear Fatigue

The goal of this study is to establish capability to predict the effect of variations in solder joint parameters such as pad metallization and chemistry, solder joint geometry, solder composition and thermal history on the microstructure, and thermomechanical behavior of various lead free solder joints. Correlations between these solder joint attributes and the ambient shear fatigue performance will be analyzed in detail. Preliminary results indicate that room temperature fatigue tests display promise as a relatively simple and sensitive means to monitor the effect of different processing parameters on solder joint reliability. It is planned to characterize the effects of load, PCB surface finish and pre-aging on various Pb free solder joint microstructures. Isothermal shear fatigue life will be measured at both ambient and elevated temperature (125˚C). The effect of prolonged exposure to high temperatures (125˚C to 200˚C) solder joint microstructure will be carefully noted, including interfacial intermetallic compound thickness and composition, as well as void formation and precipitate morphology.

MAT7H. SnBi(Ag) Low Melting Temperature Solders

Low melting temperature solder alloys are being considered for assembly of telecom infrastructure equipment that requires highly temperature sensitive components such as optical transceivers. In this project several low melting temperature solder alloys will be selected for process and reliability evaluations. SnBi, SnBi(Ag), or SnIn alloys will be considered. The mechanical robustness of these alloys are known to be suspect, especially under high strain rate loadings. Drop shock performance will therefore be the primary means of evaluation. Other reliability test methods such as thermal cycle will be considered as follow on tests for promising alloy candidates.

MAT8B. Conformal Coating: New Materials and Methods

Conformal coating of circuit board assemblies have long been used for protecting components and circuitry from harsh environmental conditions. While these coatings may serve to mitigate both corrosion failure and Sn whisker shorting risk, their impact on other reliability failure risks such as thermal fatigue of solder interconnects is not well known. The AREA Consortium has been exploring the interconnect reliability consequences of popular conformal coatings since 2013. These studies have looked alternately at SAC305 and SnPb eutectic solder connections with a variety of conformal coating materials. The 2014 AREA program included a detailed study of SnPb solder joint fatigue in conformally coated boards with range of different package types. Humiseal, Arathane and Parylene coatings were studied. The reliability impact of the coating was found to be sensitive to the package standoff height for the various Bottom Terminated Components on the board. Most recently (2015), SAC305 assembled boards were coated with UV curable polyurethane coatings, Humiseal UV40 and UV50. These test boards (TB2015) are now being cycled at (-40 to 125°C). Testing will continue into 2016 until sufficient fails accumulate. Included also are boards with a new plasma nanocoating, Semblant SEM400.

In 2016, UV40 coated boards will also be tested with an alternate thermal cycle (perhaps -20 to 80°C) to explore the effect of coating on the thermal fatigue acceleration factors. Uncoated TB2015 boards will be included as controls. 2016 will also include a follow up investigation of thin coating (SEM400, Parylene C) impacts on the reliability of SMD resistors.

MAT8C. Component Rework with Conformal Coating

Military/Aerospace equipment providers commonly use conformal coating to protect assemblies from harsh environments. These applications are often defined to survive for considerable time in the field. Given high cost and low production volume of these assemblies, there is often need to replace individual components on boards returned from the field (upgrades, failures, redesigns). Critical assessment of such rework is rarely included in the original product qualification. It becomes a program necessity years later. The reliability consequences of such rework are therefore poorly understood.

Using the TB2015 vehicle, select components will be removed from coated boards, new components

reattached, and the site re-coated. These vehicles will be resubmitted to thermal cycle testing to determine the reliability consequences of the rework operation.

MAT9: Filled Polymer Electrical Interconnects

Conductive adhesives and other filled polymer systems provide an alternate (and lead-free) method of electronic interconnect. Such materials have a long history of use in low cost consumer goods where product design life is relatively short and reliability expectations modest. They typically produce relatively high impedance interconnects, but can nonetheless find application in higher grade electronics where very low assembly temperatures are an absolute necessity.

MAT9A. Conductive Filled Elastomer Connections

Many high performance optoelectronic components such as optical transceivers cannot tolerate the typical assembly temperatures required for modern lead free circuit board assemblies. Some may be limited to process temperatures as low as 80°C. This project is exploring some interconnect options for such temperature limited components. A first material to be evaluated will be a conductive filled elastomer connection system supplied by one of the consortium Principals. It is designed for use with a compression socket in an area array format. Connection between component and board is provided by metal spheres embedded randomly in an elastomeric interposer. Socket compression enables local conductive paths along contacting metal spheres in the matrix.

The integrity of the electrical connection provided through the elastomer interposer will be evaluated through exposure to a harsh thermal cycle (-40/125°C). Of equal importance will be the stability of the insulation resistance maintained between nearest neighbor contacts during elevated temperature and humidity exposure (85%RH/85°C). Detailed material characterization and construction analysis will also be done. The extent to which other ECA materials can be evaluated will depend on interest and materials supplied by the Principals.

Reliability

The AREA Consortium investigations into packaging reliability are more fundamental than simply testing assemblies under pre-defined conditions using standard test procedures. Our Principals often require standardized accelerated life testing for product qualifications. These methods are typically intended to evaluate product designs and material selections but there is often limited understanding of the role assembly process variables may play in the final product reliability. The AREA Consortium takes a more

holistic approach, considering the contributions of test methods, design, materials and assembly process variables to the overall reliability observed under various stress conditions. The projects described in this section have been defined in consultation with our Principals and are intended to improve the understanding of the reliability consequences of various product and process attributes and, in some instances, the impact of test methodology as well.

REL3C. Random Vibration Testing

Previous efforts with newly installed vibration testing apparatus focused on fixed frequency vibration testing with resonance tracking and proper monitoring of electrical failures during vibration. Such fixed frequency loading is most suited for scientific investigations of vibration induced failures in solder interconnects. However engineering specifications that define vibration testing for electronic product qualifications more often specify random vibration loadings. Using a similar test board design as previously tested with fixed frequency testing, this project will explore the response of common lead free solder interconnects to random vibration loading.

Other enhancements to the vibration testing apparatus such elevated temperature testing capability will also be explored.

REL6A. Solder Paste Print Correlations to Reliability

Variability in the volume of individual screen printed solder paste deposits is a fact of life in SMT assembly manufacturing. Decisions as to whether to reject local instances of low paste volume are made routinely on the production line. These decisions can be made based on operator judgement or through fixed criteria programmed into the automated solder paste inspection (SPI) tool. The actually consequences of proceeding with undersize or oversize deposits is rarely experimentally determined and such acceptance criteria are often arbitrary. An acceptable solder joint can be defined alternately as one that successfully joins the two surfaces to be mated or one that provides an interconnect with acceptable reliability for the application of interest. This project explores both.

A key element of this effort is an understanding of stencil print process window sensitivity for various package types based on the statistical analysis of SPI results. A first phase has explored the limits of paste volume for successful solder joint formation at low volume deposit locations. A second leg of the experiment now underway is evaluating the effects of individual paste deposit variability on the thermal cycle reliability of BGA, LGA and other package types. Similar to the assembly yield study, solder prints have been produced which will contain one or two intentionally oversized or undersized deposits strategically located at joint locations which are most likely to fail in thermal cycling. These outlier deposits are sized such that their volumes are outside typical allowable tolerances (±50% or more). Such samples have been assembled and are being thermally cycled. Failure times and locations will be

compared with those of baseline assemblies having nominal solder joint dimensions throughout to determine if a single large or small paste deposit can measurably impact the interconnect reliability for any given component type.

REL9A. VIPPO (Via-In-Pad, Plated Over) and other Via Design Considerations on BGA Reliability

Several AREA consortium Principals are reporting problems with the inability to reliably form BGA solder connections on VIPPO pads when they're mixed with non-VIPPO pads in the same component footprint. The delay in solidification of BGA solder joints above the VIPPO structure is presumed to lead to hot tearing of those solder joints at the component interface. The specific design attributes of such mixed VIPPO/non-VIPPO footprints that lead to BGA joint separations is largely unknown.

This project will explore the BGA solder defect rates associated with various combinations of VIPPO design attributes in the printed circuit board. Features considered will include PTH dimensions, VIPPO positions relative to non-VIPPO pads, pad size, pad pitch, PTH backdrilling and the presence of mirrored BGA components. Other test board attributes are expected to contribute to the final result. PCB laminate CTE and temperature induced warpage will be important. Relatively thick test boards (>110 mils) will be used to emulate the behavior of complex network/server applications. Reflow profile sensitivity will also be explored paying particular attention to the response for top side and bottom side attach.

The primary objective will be to identify some PCB design rule guidelines for minimizing the occurrence of BGA hot tearing with various combination of board via structures. The test boards used will be sourced with at least two different laminate materials to indicate the contribution of laminate properties on the design rules obtained. Follow-on investigations of other common via structures such as blind or buried via is anticipated.

REL12A. Fine Pitch Cu Pillar Interconnect for 2.5D Packaging

2.5D packaging integration technologies (multiple die on a common interposer) are of growing interest in the electronics industry. This technology has been convincingly demonstrated by several firms using silicon based interposers. The improved electrical properties and reduced cost of glass interposers however are proving to be increasingly attractive to designers. Experimental demonstration of glass interposer technology is quite scarce though. A collaborative project with several key industrial partners is underway to study the ultra-fine pitch metallurgical interconnect between silicon die and glass interposer. Silicon wafers have been bumped with solder capped fine pitch copper pillars, diced, and assembled to circuitized glass interposers in the APL. Metallurgical analysis is being performed on the resulting copper pillar joints of varying sizes and pitches down to 50 microns. Of particular interest will be the consumption of solder into intermetallic compounds in fine scale joints. Reliability of these fine pitch interconnects will be evaluated. Thermal cycle and drop shock stresses are being explored.

REL13A. Compliant Pin Connections

Compliant (or press fit) pins are being increasingly used in complex assemblies to avoid difficulties with solder holefill and thermal board damage encountered with Pb-free wave soldering of thick printed circuit boards. A proliferation of high speed, microcompliant pin connector designs are also finding application for smaller, high speed cards. The effectiveness of these PTH connections is intimately dependent on the diameter of the drilled hole, the plated copper thickness and the surface finish of the PTH wall. Pin insertion force and retention force are attributes commonly used to gage, respectively, the damage to the surrounding laminate material and the mechanical robustness of the electrical connection. This study will explore the sensitivities of PTH physical attributes to press fit loads and laminate strains through numerical simulations. Select cases will be confirmed through experimental pin insertions and extractions using a member supplied pin structure and circuit board material. Laminate damage will be characterized when observed.

A second phase of this effort will experimentally compare the insertion/retention response of immersion tin surface finish to an OSP finish for some fixed set of PTH attributes.

REL15A. Power Cycle Reliability Test Method

Common thermal cycle reliability tests of electronic hardware are recognized to be a simplification of the stress gradients imposed by functional operation in the field. Heat dissipated from a powered device produces a temperature gradient which adds additional stresses to package interconnects over and above those arising from simple CTE mismatch. Moreover, the cycle ramp time is much shorter than that which can be imposed by a large environmental test chamber. Instrumentation for powering test circuitry directly with arbitrary waveforms now resides in the AREA laboratory. Initial power cycling method development will be performed on simple nets of board mounted SMT resistors heated to a fixed peak temperature. Solder interconnect reliability of these small devices in power cycle will be established through in-situ monitoring of the resistor test nets.

REL15B. Power Cycle Reliability of QFN Packages

Wirebond QFN packages are being fabricated with resistive test die for power cycling evaluations using the test method defined above (REL15A). The package is a single perimeter row 12.0 x 10.5 mm body and 0.4mm lead pitch. Each die contains eight resistive elements to emulate functional hot spots on a die. Power will be dissipated in a realistic fashion through the soldered thermal pad of the QFN body. The reliability of solder interconnects will be monitored for the duration of the power cycling test.

REL16A. Die Size Effects on the Reliability of BGA Package Interconnect

Amkor 192 I/O CABGA packages will be used to measure the effect of silicon die size on board level

solder joint reliability. BGA interconnects will be of the commonly used SAC305 alloy. Otherwise identical components have been obtained with die sizes of 12, 9.5 and 7.2mm square. Two thermal cycle profiles (0/100°C and -40/125°C) will be included to reveal die size effects on thermal fatigue acceleration factors. Components have been allocated for characterization of temperature induced warpage at each die size. Predictive model development using these thermal cycle results is planned.

Assembly Process Development

By virtue of its access to surface mount manufacturing equipment, the AREA consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. AREA Principals have an ongoing need to refine manufacturing process windows and identify design improvements that can be implemented to improve yields for products of ever increasing sophistication. Successful introduction of new technologies at high yield, requires thorough up-front process development often to levels not anticipated in new product introduction budgets.

Assembly data and observations for every component that is investigated, characterized, assembled, and tested, is uploaded to the AREA Component Database for easy and quick access in addition to the final project reports (http://www.uic-apl.com/databases).

APD1A. Broad Band Paste Printing

Fine scale packages and passive devices developed for the space constrained, consumer handheld market are increasingly finding application in complex server/telecom boards. Performance requirements often dictate their board placement in close proximity to substantially more massive SMT components. The solder paste printing parameters required for coarse featured components often limit the resolution of paste prints for the nearby fine feature components.

A test board was designed for evaluating the printing quality of fine components immediately adjacent to a relatively coarse featured 55 mm square 1 mm pitch BGA. The fine feature components include small passive devices, WLCSPs and small QFNs down to 0.35 mm pitch. These test boards were assembled after numerous print optimization trials.

The 2016 phase of the project consists of paste printing trials only. Design variations of the previously assembled BGA/WLP/QFN cluster include reduced component proximity, orientation changes and elimination of white ID markings. Printing trials will be run with a variety of stencil thicknesses and

stepped patch configurations. The resulting print quality for the fine feature sites will be monitored using both visual inspections and automated paste inspection tools. Conditions producing inadequate print quality will be noted in order to provide design guidance for manufacturable component placement.

APD1B. Paste Printing SPI Calibration

High yield SMT assembly of complex product depends critically on Solder Paste Inspection (SPI) using state of the art paste deposit measurement systems. Such tools monitor screened paste deposit volume in production to flag anomalous prints prior to component placement. These measurements are typically used to provide relative comparisons to prior prints known to produce acceptable assemblies. The absolute accuracy of the paste volume data will depend both on the method of measurement (*i.e.*, how the surface of the paste is detected) and the sophistication of the volume calculation algorithm. For instance, a simple calculation of maximum deposit height times the deposit area would be prone to overestimate the total paste volume if the deposit takes some characteristic peaked shape rather than the assumed flat top shape. This project will explore experimental options to measure the accuracy of paste volume measurements on a high throughput production SPI tool.

APD3B. Large Body BGA Characterization

As the need for bandwidth grows unabated, ever expanding I/O counts drive very large body size substrates for the packaging of high performance processors and complex ASIC and FPGA die. Laminate substrate body sizes up to 55 mm are not uncommon in the enterprise server and network telecomm space. A common structure consists of a substrate with several buildup layers on a laminate core, a flip-chip attached die, and a metal heat spreader lid attached to the substrate with a perimeter adhesive and in thermal contact with the silicon device through a thermal interface material on the back of the die. The temperature induced warpage of this package structure is critically dependent of the properties of the materials selected for its construction. Given the large area footprint of such packages, the board assembly yield and interconnect reliability are in turn highly sensitive to that resulting warpage.

This project is a case study of large body BGA packages using representative materials as defined by interested member companies. Large body (55x55mm) flip-chip packages will be fabricated using thin core (600µm) laminates and coined copper lids. Warpage behavior will be characterized for a variety of die sizes, including at least one multi-die configuration. A comparison will be made between the responses of two different thermal interface materials (putty or grease formulations). The BGA interconnect thermal cycle reliability will also be measured as assembled to an appropriately thick (0.125”) circuit board.

APD9A. Warpage Contribution to Head on Pillow Defects

Higher solder melting temperatures and reduced wetting capability of Pb-free solders have dramatically increased the occurrence of Head on Pillow (HoP) BGA soldering defects. This defect is characterized by a BGA solder ball lifting out of its intended solder paste deposit prior to solder melting due to temperature induced distortion of the package or circuit board. The BGA ball drops back into the solder on the board during cool down but does not wet to that now molten solder deposit and form a coherent joint. For a fixed set of solder materials and reflow profile, the incidence of HoP defects is expected to depend on the magnitude of temperature induced (or 'dynamic') warpage. The dynamic warpage characteristics of BGA packages are often such that a solder ball grid array which is nearly flat at room temperature will be distorted considerably out of plane at solder solidification temperatures.

A more fundamental experimental approach to understanding this phenomenon will be taken in 2016. Previous investigators have shown that BGA balls suspended above a melting solder paste deposit can still be wet as the deposit melts. The physical separation distance however must be quite small. The separation distance beyond which wetting can no longer reliably occur is speculated to be a direct indicator of the maximum warpage that can be permitted without encountering Head on Pillow defects. A side view camera for the BGA rework tool has been purchased to directly observe this suspended BGA wetting phenomenon. Assembly material variables such as paste flux formulation, mesh size, ball alloy and ball diameter can be evaluated directly in this manner.

APD9B. BGA Socket Warpage Evaluations

Because of their large body size and injection molded housing construction, hybrid BGA sockets can prove particularly problematic for warpage induced assembly defects during board attach. These include solder joint opens and Head on Pillow defect (contact non-wets). Using member supplied BGA connectors (sockets), warpage response will be measured with available methods. Techniques that monitor full BGA array in a non-destructive manner will be of particular interest.

APD10A. Fine Pitch Package on Package Assembly

A common approach to Package on Package assembly is a pre-stacking of components before final board assembly. This approach enables convenient scrapping of defective PoP stacks before board assembly but requires the added cost and reliability impact of an extra reflow step. This project will investigate a Package on Package assembly process in which components are stacked directly on the board and joined with a single reflow rather than pre-stacking. The process shall be defined using a 0.35 mm pitch wirebond package stacked on a larger I/O 0.4 mm pitch flipchip BGA package. Of interest will be the optimum BGA ball size at each level for both process yield and PoP reliability. Test board pad design attributes will also be considered.

Consortium Deliverables

The charter of the AREA Consortium is to convey the body of research performed and knowledge acquired directly to the Principals in a practically useful manner. This is achieved by providing information in various formats and transfer means including technical seminars, accessible databases, written reports, process recommendations, as well as design guidelines and testing protocols.

Reporting of Results

The AREA manager and staff will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings, with audio commentary, will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Project needs may require the AREA staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.