# AREA Consortium

Dear Members,

Our fall project review meeting was held earlier this month on the Binghamton University research campus. In addition to our usual staff and student project updates, the agenda also showcased some collaborative activities with our member companies on varied topics such as conformal coating corrosion protection, fine pitch solder paste printing and lid adhesive selection impact on BGA package warpage.

Several 2015 projects were closed out at the meeting. Dr. Kondos presented final reports on the two recently completed laminate pad cratering projects: MAT2C *High Tg Laminate Materials* and MAT2D *Cu Foil Roughness Effect* while Dr. Schoeller closed out the BGA compression study, REL11A. New research projects were also formulated. A team of interested member companies convened after the formal meeting to define critical attributes of the soon to start Large Body BGA project.

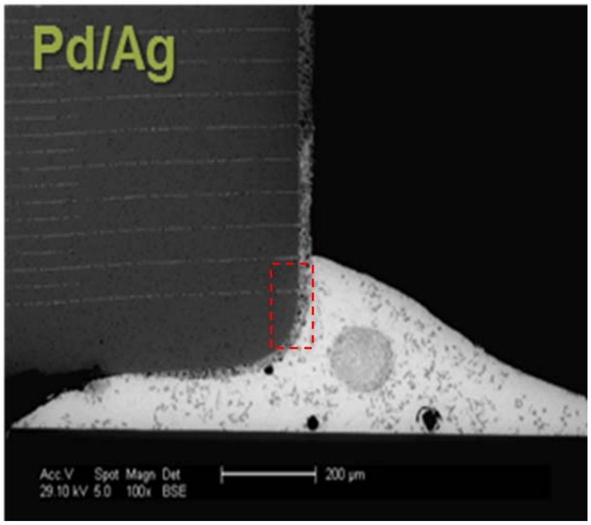
Presentation charts for the fall meeting are posted on the AREA website for member download. Audio commentary files for these presentations will be included shortly.

Sincerely,

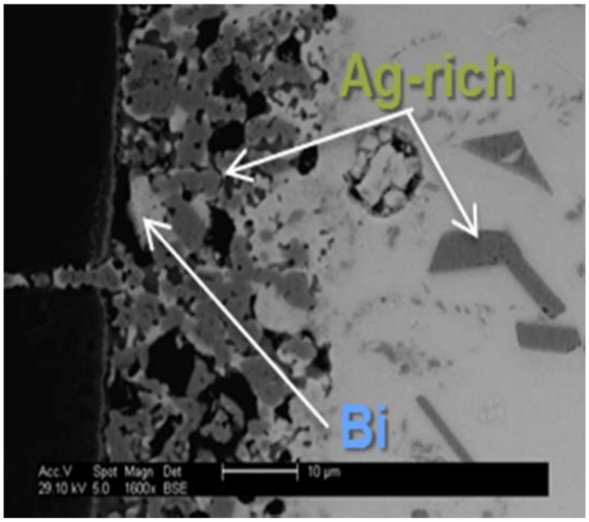
Jim Wilcox
Consortium Manager

**MAT6D. Passive Device Surface Finish**

The passive device surface finish project is evaluating various SMD interconnect options for high temperature capacitors to be used in elevated temperature applications. Devices with five different surface finishes have been assembled using four different high temperature interconnect materials. The microstructure and interfacial reactions were analyzed for each combination. These observations were reported at the recent fall consortium meeting for joints in the as-reflowed or as-cured state. Room temperature device shear tests were also performed and the fracture surfaces analyzed to identify the failure mode. Future work includes high temperature device shear and thermomechanical reliability testing.




*BiAgX solder joint on PdAg surface finish device.*




*High magnification image of interface region.*

## Alternate Lead-free Solder Alloys

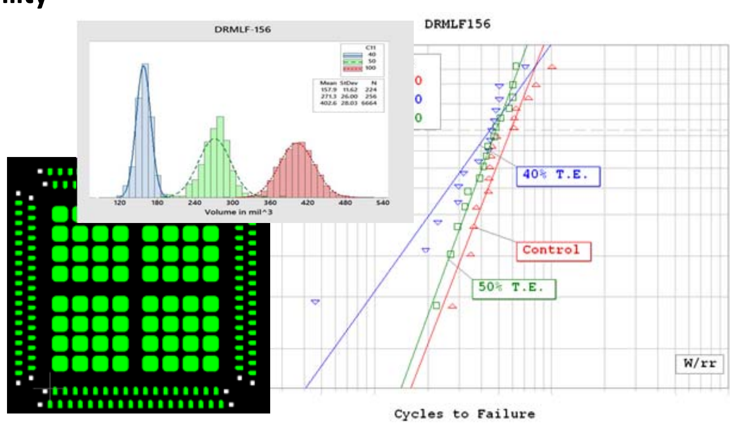
An extensive experiment is underway to evaluate the thermal fatigue reliability of various Pb-free solder alloys (MAT7E and MAT7F). The ATC performance of several new alloys (such as Innolot, Violet, and two other SnAgCu based alloys microalloyed with Bi and Sb) will be compared to that of the common SAC305, SAC105 and eutectic SnPb solder alloys. Both ENIG and Cu-OSP finish boards are being used to investigate the effect of board surface finish on microstructure and subsequent reliability of solder joints. Approximately 320 test boards were assembled using different reflow profiles appropriate to the alloy in question. Solder paste and ball alloy compositions were matched to avoid solder composition change at assembly. 100% paste volume measurement was performed to enable correlation of reliability to processing parameters. ATC testing using three different profiles (-40/125°C, 0/100°C and 20/80°C) will start soon. The effect of thermal preconditioning (aging) will be examined on some select alloys. Detailed solder joint microstructural analysis of as-assembled and failed samples is planned.


*Assembled TB2015 test board used in the alternate alloy study; various LGA, BGA and MLF package types are being tested.*


*Bright field image of a 10 mil solder ball of the 'Violet' alloy composition (Sn2.25%Ag0.5% Cu6.0%Bi) on an ENIG surface board.*

## REL6A. Solder Print Correlations to Reliability

The reliability consequences of discrete instances of low volume paste print deposits are being investigated. Intentionally undersized stencil apertures are placed at strategically chosen high risk locations in the component footprints of various package types to force printing 'outlier' deposits. Thermal cycle reliability results on such assemblies are now coming in to quantify the effect of these underprints on interconnect reliability.

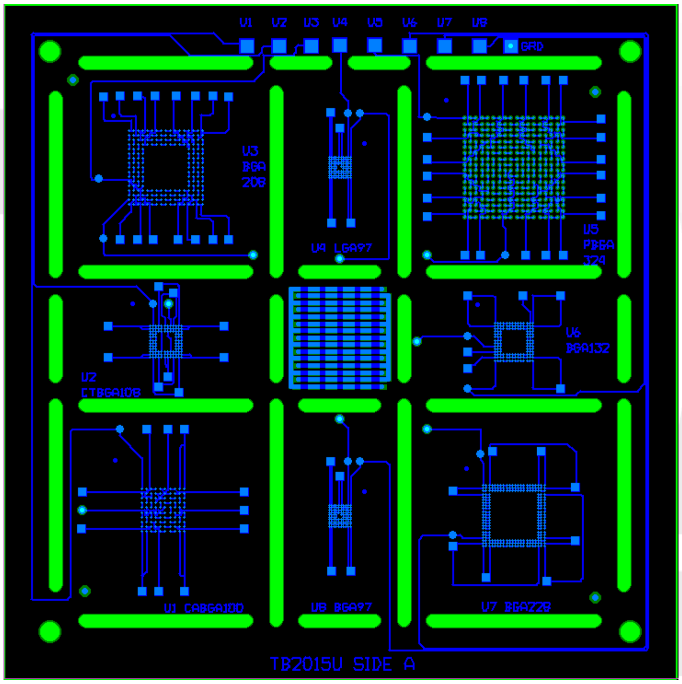



*Dual-row MLF example of forced outlier deposits: Corner pads (white) are printed at 40% and 50% nominal volume.*

**MAT1B. Reworkable Component Underfills**

Accelerated thermal cycling of the first three sets of TB2014U assemblies continues (underfill materials E and F along with the no underfill baseline). Many parts have failed. As expected, the failure rate varies widely depending on the component type and the underfill material. Some combinations have already achieved 100% failure while others have yet to see a single failure. The first failures of all failing combinations have been removed, cross-sectioned, with the solder joints and laminate under the pads being examined for cracks. The two latest underfill materials (G and H) were used to underfill the remaining two sets of assembled test boards but no cycling results for these are available at this point.

All the required reworkable underfill materials for the next stage of the project are in house and the corresponding programming of the dispense equipment for the new TB2015U test board is ongoing. An alternate test vehicle together with components and underfills contributed by a member will be used to study three additional materials.

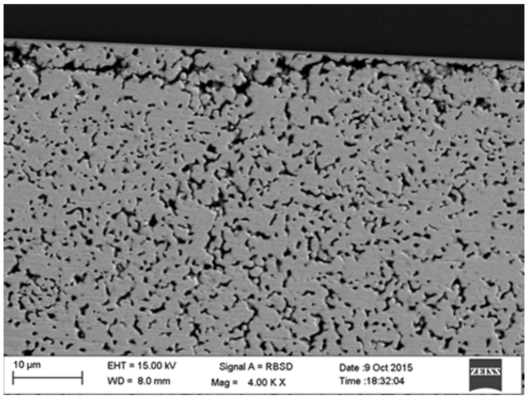



*TB2015U underfill test board top surface design.*

**MAT6B. Sintered Silver Die Attach**

A detailed study of the microstructural evolution of sintered silver die bonds during high temperature storage has been completed for both thin (<20µm) and thick bond lines (>80µm). Microstructural observations and die shear strength measurements for these structures were reported at the recent fall consortium meeting. Other sintered silver bond samples are progressing through thermal shock reliability testing. The attached image shows a typical die side failure mode imparted by -50 to 200°C thermal cycles. This experiment includes an evaluation of thermal pre-aging on thermomechanical reliability.

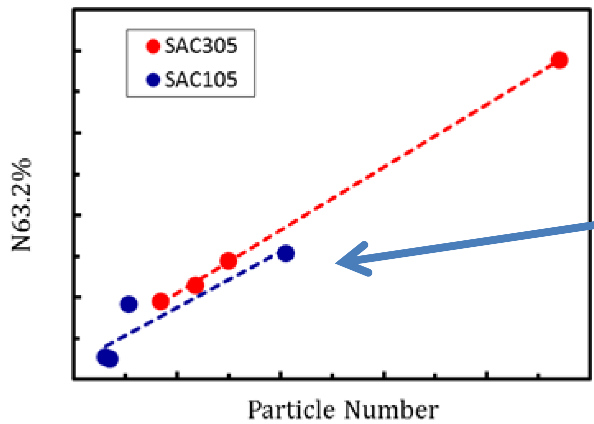
The next phase of this project will focus on process development and the effect of process parameters on thermomechanical reliability. Process parameters to be varied include sintering temperature, time, and ramp time. Package parameters such as substrate metallization, die size, and bond line thickness will also be varied. The Design of Experiment incorporating these project variables can be found in the above mentioned presentation available on the AREA website.



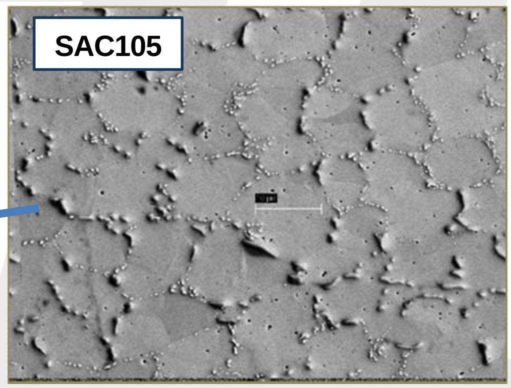

*SEM image of pre-aged sintered-Ag joint (die side) after 2000 cycles of -50˚C to 200˚C thermal shock.*

## MAT7B. Isothermal Mechanical Behavior of Solder Alloys

Ongoing isothermal shear fatigue testing of various Pb-free solder alloys has revealed some intriguing results. The shear fatigue test is found to be very sensitive to solder composition, PCB surface finish, effect of pre-aging and strain. Trends similar to those seen in thermal cycle testing were observed in the room temperature fatigue test (*e.g.,* increasingly higher fatigue lifetimes as the amount of Ag in solder is increased). Moreover, these tests have identified a linear correlation between the number density of the $Ag_3Sn$ strengthening particles and the characteristic fatigue life. This correlation may prove valuable in quantifying the effect of thermal aging on fatigue behavior of SnAgCu alloys through the kinetics of precipitate coarsening.




*Characteristic fatigue life of SAC105 and SAC305 20 mil solder balls versus number of $Ag_3Sn$ precipitate particles per unit area.*

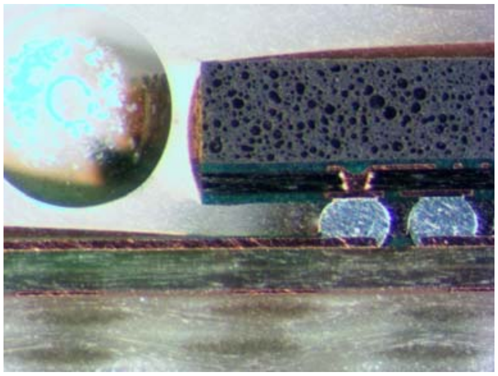



*$Ag_3Sn$ precipitate particle density in as-reflowed SAC105 solder joints*

## MAT8B. New Conformal Coating Materials

The reliability consequences of several new conformal coating materials are being evaluated with SAC305 assemblies. These include UV curable coatings Humiseal UV40 and UV50LV and plasma nanocoatings Semblant Plasmashield 200 and 400. With the thicker UV coating materials, fillets typically form around bottom terminated components (BTC) and degrade the reliability of the solder joints. Thinner plasma nanocoatings have minimal impact on BTC reliability. Thermal cycle testing continues.

*UV40 coating fully encapsulates bottom terminated components such as this QFN.*



*UV coatings fail to encapsulate higher standoff devices such as BGA and CSP components.*