ADVANCED RESEARCH IN ELECTRONICS ASSEMBLY

Consortium 2015 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium will fund manufacturing relevant research to provide an understanding of emerging technologies in materials, reliability and assembly process to AREA Principals. The research plan ranges from academic research on fundamentals to topics directly applicable to current manufacturing needs. The objective is to provide AREA Principals with meaningful data that enable sustainable assembly process improvements, maximization of yields and improved product reliability.

The AREA Consortium appreciates that our Principals have little time or resources to devote to research beyond critical product needs. Therefore Principals of the AREA Consortium are encouraged to view the consortium staff as an extension of their own engineering team, devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, including project milestones and timely research results, a comprehensive website with on-demand content is made available (http://www.uic-apl.com/).

The AREA Consortium research plan is Principal driven, consortium manager prioritized, and consortium staff executed. Research is based on current and near term future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The consortium manager and staff define the research plan in close partnership with AREA Principals and the AREA Steering Committee (http://www.uic-apl.com/home/area-steering-committee). The manager and staff execute the research plan using the resources and facilities of the Universal Instruments Advanced Process Laboratory along with adjunct university capabilities as needed.

The primary focus for 2015 will be the initiation and/or the completion of the projects outlined in this document. Additional topics are added throughout the year as materials are provided and interests develop given that resources are available. The 2015 research plan topics have been categorized into three key thrusts: Materials, Reliability, and Assembly Process Development.

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Materials

Advances in assembly materials often provide manufacturers with the means to further optimize process and increase yield. However, the breadth of available material types and the opportunities for complex materials interactions result in significant challenges in evaluating, selecting and qualifying these emerging technologies. AREA Principals are faced with evaluating the base properties of these materials, the assembly process window they require and their performance in accelerated product qualification tests. One mission of the AREA Consortium is to provide its Principals relevant and timely information on selected materials to alleviate this challenge. The AREA Consortium uses a systematic, scientific approach to perform assembly material evaluations that are both comprehensive and comparative in nature. Thorough characterizations of materials under investigation are typically included to provide a fundamental understanding of the process windows and reliability impact observed with their product use.

MAT1A. Underfills and Adhesives

This research is a continuation of the systematic evaluation of various capillary underfills for component attachments. Materials for this investigation have been acquired from multiple suppliers. Components of various designs (BGAs and LGAs) are represented on the 2013 AREA Consortium test board for use in these studies. One goal of this investigation was to provide directly applicable insight on flow characteristics and voiding under typical and low standoff components. An important consideration for each capillary underfill is its compatibility with flux residues and flow behavior. These capillary underfill materials are being subjected to reliability testing by accelerated thermal cycling. Much of the planned work for this project was completed in 2014. Final efforts to close the project in 2015 will consist of completion of thermal cycle exposures and the associated failure analysis to identify the impact of underfill material and joint encapsulation characteristics.

MAT1B. Reworkable Underfills

Interest in board level underfill materials continues to be strong among the consortium Principals. The work of evaluating the process and reliability performance of such capillary underfill materials will continue in 2015. This next iteration of board level underfill evaluation will focus on those materials marketed as thermally reworkable formulations. Materials to be evaluated will be selected in consultation with various interested Principals. Test board used will be of the new TB2014 design in order to evaluate a different set of components. Board assembly will otherwise consist of industry standard SMT processing. The common Mil/Aero industry practice of post assembly board washing will be considered as a potential process variable, if such process capability can be identified. Thermal cycle reliability with these materials underfilling the originally attached (non-reworked) component will be tested. The rework capability of these materials will also be explicitly explored. The process of underfilled component removal and site redress will be exercised.

MAT2A. Circuit Board Material

This project will be an extension of prior laminate studies that compared various board materials in terms of pad cratering using the Hot Bump Pull (HBP) technique. In addition to studying a laminate material not used in the previous studies, an additional variable will be introduced, namely the treatment of the bottom surface of the outer copper foil. The older studies had provided some evidence that smoother copper had led to stronger pads, probably by reducing the defects introduced in the laminate surface due to the copper roughness. The effect, however, had been weak, because the difference in roughness between the two types of copper was small. In the planned research, up to five different Cu foils, with a wide range in roughness, and two laminates will be considered. HBP strength tests will be conducted first, but HBP fatigue might be included later if the strength tests prove inconclusive.

MAT2C. High Tg PCB Laminate Materials

From the early days of circuit board laminate material changes in response to the introduction of Pb-free solders, the AREA consortium has been active in characterizing the robustness of new laminate materials through Pb-free reflow temperature exposure. The laminate material industry continues to make new laminate materials available for circuit board fabrication with varying combinations of dielectric loss, Tg, and decomposition temperature. In 2015, the consortium will again review the robustness of some latest industry offerings as indicated by pad cratering response in ball pull testing. Board materials to be tested include high Tg phenolic (filled and unfilled) as well as many halogen free formulations. Pad cratering in these new laminate resins will be evaluated as a function of resin content and BGA pad diameter both before and after Pb-free reflow exposure. Resulting data is to be included in the consortium laminate circuit board materials database.

MAT3A. Surface Finishes

A large number of new surface finishes have been made available to the electronics industry in the recent past. The AREA Consortium provided process and reliability comparisons for several of the common set of materials such as ENEPIG, lead-free HASL, OSP (ENTEK OM), Pallaguard, and others, in 2013. The objectives of the current study are to complete the associated thermal cycle reliability evaluations. In addition, a considerable effort in the analysis of microstructures and failure mechanisms for solder joints of various volumes and configurations has been ongoing. These results can be used by our Principals in evaluating the various failure modes associated with these surface finishes in lead-free soldering applications.

While the ATC test was completed and microstructural work on selected BGA samples were finalized and reported in 2014, further microstructural work on other select components (such as QFN, LGA and WLCSPs) will continue in 2015.

MAT4B. Thermal Characterization of Putty Thermal Interface Materials

As logic speeds continue to increase the need to remove heat from high end electronics is becoming more of a challenge with standard TIMs. In addition, material degradation in field is a significant risk for the performance of electronics expected to remain in field in excess of 20 years. This research intends to evaluate several putty materials from multiple suppliers using the component level TIM tester developed in 2012. The project will be divided into two parts, process development and thermal characterization. A deposition process will be developed for each material using an Asymtek™ dispenser. Materials will be characterized at time zero with a fixed bondline thickness and after high temperature storage. Time permitting, assembles will be thermally cycled to evaluate "pump out" risk.

MAT5A. Paste and Flux Printing Evaluations

A protocol for printed paste characterization was established in 2014 using typical industry standards along with automated paste inspection tools. A standardized test board representing current component technology is being used to study printability of these paste materials. The goal of this study is to characterize the effect of component pitch and pad design on print transfer efficiency. Large scale analysis of the print data collected will proceed in 2015. A print process evaluation kit with the same print test board design as used above on the APL line has been prepared to enable direct comparison with similar process characterizations at member company screen printing operations.

High Temperature Electronics Research Overview

As electronics become integrated into higher temperature environments such as those associated with deep well drilling and distributed controls in the automotive and aviation applications, higher melting temperature solder alternatives are needed. In 2015 the program will continue to focus on the materials, assembly, and reliability of high temperature electronics packaging. A new high temperature polyimide test board will be designed for the following projects.

MAT6B. Die Attach and New Pb-free Alloys

High temperature die attach materials are mission critical for the operation of next generation wide band gap semiconductor devices for power applications. These products operate at substantially higher temperatures than conventional electronics. With current Restriction of Hazardous Substances (RoHS) exemptions expiring, it is imperative to consider Pb-free alternatives for such high temperature applications. The focus of the study will be a continuation of joint level strength, reliability, and microstructure evaluations. Various types of die attach materials will be studied and characterized for their viability as drop-in replacements for current materials. The materials to be investigated include alloy pastes, sintered pastes, metal filled epoxies, and new Pb-free alloys developed in conjunction with

Binghamton University. Thermal shock testing of these candidate attach materials will continue to failure in 2015. Work will include thermal characterization of these joints.

MAT6E. Effect of Passive Device Surface Finish on Thermomechanical Reliability in High Temperature Applications

The AREA consortium has extensive experience evaluating surface finish effects on active component solder geometries such as BGA or LGA. Component surface finish effects with small passive devices are relatively unknown. The surface area on the passive device relative to its solder joint volume is often quite large such that the surface finish could have outsized effects on the resulting joint metallurgy and interconnect reliability. The case of high temperature applications may exaggerate the metallurgical impact of surface finish yet further.

This project will study how passive device (capacitor) surface finish affects interfacial reactions, microstructure, and mechanical behavior of solder interconnects used in high temperature electronics. The project scope will include the development of a high temperature reflow assembly process on a high temperature (polyimide) test board and measurement of solder fatigue lifetimes under extreme thermal cycle (-50C to 200°C). Metallographic analysis will link microstructural observations to observed mechanical behavior and fatigue performance.

Various candidate solder alloys will be evaluated with Alloy 151 (Pb5Sn2.5Ag) being the control composition. Capacitors will be provided by an industrial partner with various surface finishes. A common surface finish, 85Pb15Sn, will be the control finish.

MAT6F. Evaluation of Pb-free Alloys for Under the Hood Applications

The ROHS exemption for Pb in high temperature solders will be reviewed again in 2016. In anticipation of the eventual elimination of Pb in high temperature solders, there is a need to find Pb-free alloys that can withstand the high operation temperatures encountered in under the hood applications up to 200˚C.

This work will study the microstructure evolution and thermo-mechanical reliability of several new Pb-free alloys in high temperature environments. The test vehicle will consist of several different types of components including but not limited to BGAs, QFPs, and surface mount resistors. Potential alloys will first be screened through a combination of high temperature storage and shear tests with various simulated maximum operating temperatures (150°C, 175°C, 200°C). The room temperature/ high temperature shear strength will be analyzed in the context of microstructural evolution and interfacial intermetallic growth behavior. After screening out poor performers, the thermo-mechanical reliability will be studied through high temperature thermal shock tests. New alloys will be compared to high-Pb and Innolot controls in terms of characteristic lifetimes, and failure mechanisms. Microstructure analysis will be used to help interpret lifetime trends and observed failure modes.

MAT6G. Intermetallic Growth Kinetics on Electrolytic Ni in High Temperature Environments

RoHS legislation coupled with extended temperature ranges for conventional electronics necessitates the study of standard temperature Pb-free interconnects at temperatures up to 200˚C. At higher operating temperatures solders can experience extensive precipitate coarsening, grain growth, interfacial intermetallic compound (IMC) growth, and interfacial defects such as interdiffusion voids. This work will focus on the intermetallic growth kinetics of Ni_3Sn_4 on electroless and electrolytic Ni in SAC305 solder joints exposed to high temperature environments. The microstructure evolution and intermetallic growth kinetics will be systematically studied in the temperature range of 125˚C to 200˚C. This work will provide guidance for surface finish selection when conventional interconnects are used in high temperature environments.

Lead-Free Solder Alloy Evaluations & Microstructure

Lead Free alloys with various concentrations of dopants are currently being evaluated by the industry as drop-in replacements to the standard SAC305. Suppliers claim that dopants in these alloys result in improved drop test performance along with lower material costs due to reduced alloy silver content. Our previous results have shown that mechanical and thermal reliability improvements can be correlated to microstructural differences created by varying solder volume and PCB surface finish. Significant effect of solder volume and composition on microstructure and thermomechanical performance of various lead free solder joints was observed.

This study is a continuation of the evaluation of microstructure and mechanical properties for various solder alloys on different pad finishes. This work encompasses characterizations for both individual solder balls as well as components assembled onto test boards for true second level reliability comparisons, either by ATC or mechanical testing. Another objective of this work is to quantify the performance of new lead free solder joints relative to common SAC 305 and SnPb alloys. Included in this work are SnPb controls and a mixed solder technology build consisting of lead-free solder joints and SnPb paste.

MAT7B. Effect of Reflow Profile on Mechanical Properties of Various Solder Alloys

Our results have shown that room temperature fatigue tests display promise as a relatively simple and sensitive means to monitor the effect of different parameters on solder joint reliability. It is possible to see the effect of solder composition on shear fatigue performance and correlate it to results obtained from ATC tests. The focus of research in this area of study is threefold. First, a controlled investigation studying the effect of solder joint composition and thermal history, including peak reflow temperature, time above liquidus and cooling rate, on fatigue life time of solder joints will be performed. Second, fatigue characterization of these solder joints will be conducted at room temperature as well as at high

temperatures. Third, the effects of PCB surface finish and solder volume on fatigue life time will be investigated. The overall objective of this investigation is to elucidate the reasons for early failure of joints in test. This investigation may additionally provide guidance on how process parameters are optimized to obtain more reliable solder joints. Results obtained to date have been documented in AREA reports. The study will continue in 2015 as we have received further alloys and we have started to test solder bumps reflowed on ENIG finished substrates. Isothermal fatigue test at high temperature, 125°C, will be conducted.

MAT7D. Drop/Shock Reliability of BGA and LGA Solder Joints with Various Pb-free Solder Alloys

A substantial effort is underway to understand the effect of solder volume, composition and PCB surface finish on drop shock performance of lead free solder joints. A new test board was designed based on the recommendations from JEDEC drop committee. Five different lead free alloys (including SAC-M, SN100C and Innolot) were used to assemble LGA and BGA components on Cu-OSP and ImmAg surface finished boards. Drop testing of all candidate alloys assembled to Cu/OSP boards was completed in 2014. Drop testing will continue through 1Q2015 in order to evaluate these same alloys assembled to immersion Ag finish boards. Characteristic drop/shock life will be measured and a detailed microstructural analysis of all alloys soldered with the immersion silver finish will be performed.

MAT7E. Surface Finish, Solder Volume and Mixed Alloy Effects on Thermal Cycle Reliability

The continuing decrease in the size of components brings new reliability challenges as the microstructure of lead-free solder alloys is significantly affected by solder volume and composition. It is well known that the microstructure of solder joints greatly affects the reliability of electronic package interconnects. In this work we plan to analyze the effect of PCB surface finish on microstructure and reliability of BGA and LGA samples in accelerated thermal cycling test. The effect of PCB surface finish (Cu-OSP and ENIG) and solder volume on Sn grain morphologies (beach ball or interlaced) is investigated. The failure mechanism of both LGA and BGA samples will be studied in the ATC test. In addition to common SAC alloys such as SAC 305, SnPb and mixed alloys (SAC 305 spheres +SnPb paste) will be evaluated.

MAT7F. LGA Reliability of Different Solder Alloys in Accelerated Thermal Cycle

Thermal cycle reliability of Land Grid Array (LGA) interconnects when attached with various lead free solder alloys will be evaluated in this consortium project. Various commercial components will be assembled in the form of LGA using multiple Pb-free alloys including at least one candidate low melting temperature alloy. A eutectic SnPb solder connection will be included as a control. It is planned to perform the ATC test at two different thermal cycling profiles (0 to 100C and -40 to 125C). Solder void levels will be carefully characterized to look for correlations with the rate of fatigue damage.

MAT8B. Conformal Coating: New Materials and Methods

Conformal coating of circuit board assemblies have long been used for protecting components and circuitry from harsh environmental conditions. As various military and aerospace electronics applications are forced by the supply chain to use more Pb-free component finishes, conformal coats are seeing increased use for Sn whisker mitigation as well. While these coatings may serve to mitigate both corrosion failure and Sn whisker shorting risk, their impact on other reliability failure risks such as thermal fatigue of solder interconnects is not well known. The 2014 AREA program included a detailed study of solder joint fatigue in conformally coated boards with range of different package types. Humiseal, Arathane and Parylene coatings were studied, with some cells including component dams prior to coating. The ability of the coatings to seal off the solder joints was in many instances dependent on the underfill gap between the perimeter of the component and the underlying circuit board. The test board used in 2014 was populated with small underfill gap parts (<75um) and large gap parts (>130um). A follow on will also explore the behavior of component in the midrange gap.

The industry has witnessed in recent years the introduction of a range of new coating application methods and coating materials. Assuming continued contributions of coating services by interested Principals, 2015 efforts will evaluate the reliability impact of new coating materials (eg, UV50 or CCA30 ultrathin plasma coat). Test boards can be designed and assembled in the APL but, at present, washing and coating operations must be coordinated with and executed by participating Principals to proceed with this follow on study. Consistent with Mil/Aero practice these boards will use a SnPb assembly process.

MAT9A. Electrically Conductive Adhesives

Conductive adhesives provide an alternative (and lead-free) method of electronic interconnect. These materials have a long history of use in low cost consumer goods where product design life is relatively short and reliability expectations modest.

Some of the newest high performance optoelectronic components such as optical transceivers cannot tolerate the typical assembly temperatures required for modern lead free circuit board assemblies. Some are limited to process temperature exposures as low as 80C. This project will explore some interconnect options for such temperature limited components. A first material to be evaluated will be an anisotropic adhesives supplied by one of the consortium Principals. It is designed for use with a compression socket in an area array format. Connection between component and board is provided by metal spheres embedded randomly in an elastomeric interposer. Socket compression enables local conductive paths along contacting metal spheres in the matrix.

The integrity of the electrical connection provided across the connector array will be evaluated through exposure to environmental stressors such as harsh thermal cycle (-40/125°C) and elevated temperature and humidity (85%RH/85°C). Of equal importance will be the stability of the insulation resistance

maintained between nearest neighbor contacts. Detailed material characterization and construction analysis will also be done. The extent to which other ECA materials can be evaluated will depend on interest and materials supplied by the Principals.

Reliability

The AREA Consortium efforts into reliability are more fundamental than simply testing materials under certain reliability test procedures and conditions. Our Principals are often forced into situations where accelerated life testing is a requirement. The majority of descriptions for these methods are incomplete. In addition, little data exists for the assembly and design aspects of the test that results in the greatest effect on the reliability. The AREA Consortium has developed a fundamental understanding of reliability, test methods and material behaviors under various stress conditions. The projects described in this section are, as a result of our Principals requests, to better understand both the test methodology and the failure modes generated while quantifying their impact on reliability.

REL3B. Vibration Testing

2014 AREA research efforts optimized the instrumentation and methodology for fixed frequency vibration testing of SMT electronic assemblies. A resonance frequency tracking system was designed and demonstrated to accommodate the phenomenon of laminate softening during vibration testing. Instrumentation was assembled to use four point probe event detection for higher resolution capture of electrical failures during vibration. The test method experimentation required for this prior project used boards assembled with either SnPb eutectic or SAC105 solder and consequently generated meaningful reliability data for these solder alloys in both BGA and LGA formats. In 2015, this same vibration test methodology will be used to test the vibration reliability of similar samples assembled with other solder alloys of interest to our Principals. Early experimental cells are expected to include SAC305 or mixed solder (SAC305 + SnPb paste) assemblies.

REL6A. Print Correlations to Reliability

The Advanced Process Laboratory is equipped with state-of-the-art solder paste inspection (SPI) technology. Utilizing this capability, all AREA consortium PCB assembly based projects that include stencil-printed boards will be characterized by this tool. A comprehensive collection of paste volume, area, and height data has been collected in recent years of APL production. In those instances where reliability data is collected from these assemblies, failure trends may be analyzed and correlated to the stencil printing volume measurements. The goal of this initiative is an understanding of stencil print process window sensitivity for various classes of devices based on the statistical analysis of SPI results.

A second leg of the experiment will evaluate the effects of individual paste deposit variability on the

thermal cycle reliability of BGA, LGA and other package types. During this experiment the APL will produce solder prints which will contain one or two intentionally oversized or undersized deposits strategically located at the solder joint positions which are most likely to fail in thermal cycling. The oversized and undersized deposits will be sized such that their volumes are outside typical allowable tolerances (perhaps ±50%). The samples will be thermally cycled until failure with the failure times and locations being compared to those of baseline assemblies having nominal solder joint dimension to determine if a single large or small paste deposit can measurably impact the interconnect reliability for that component type.

REL11A. Compression of Second Level Interconnects and its Effect on ATC Reliability

The thermal performance of certain types of thermal interface materials (TIMs) is pressure sensitive. Previous consortium research has shown the thermal resistance for gap pad materials decreases with increased pressure. The rule of thumb is 30% TIM compression provides a good tradeoff between increased thermal performance and acceptable component reliability. However the relationship between this TIM compression loading and the interconnect reliability of the underlying BGA component is not fully understood.

Active devices in high speed products that require thermal dissipation through large heat sinks are often placed under considerable compressive loads. A new BGA test structure was designed in 2014 to evaluate the reliability consequences of this compression load on second level BGA solder joints. Samples of this test vehicle built with SAC305 solder balls are now in thermal cycle test at varying levels of superimposed compressive loads to evaluate fatigue lives. Fatigue results will be available for analysis through 1Q2015. Metallographic analysis of BGA solder joints (failed and otherwise) will identify metallurgical consequences of thermal cycling under compressive load.

REL12A. Fine Pitch Cu Pillar Interconnect for 2.5D Packaging

2.5D packaging integration technologies (multiple die on a common interposer) are of growing interest in the electronics industry. This technology has been convincingly demonstrated by several firms using silicon based interposers. The improved electrical properties and reduced cost of glass interposers however are proving to be increasingly attractive to designers. Experimental demonstration of glass interposer technology is quite scarce though. A collaborative project with several key industrial partners has been initiated within the consortium to study the ultra-fine pitch metallurgical interconnect between silicon die and glass interposer.

Silicon wafers will be bumped with solder capped fine pitch copper pillars, diced, and assembled to circuitized glass interposers in the APL. Metallurgical analysis will be performed on the resulting copper pillar joints of varying sizes and pitches down to 50 microns. Of particular interest will be the consumption of solder to intermetallic compounds in fine scale joints. Reliability of these fine pitch interconnects will be evaluated.

REL13A. Compliant Pin Connections

Consortium membership is reporting increased usage of compliant pin connections as the preferred interconnect for through hole components. Compliant pins are used in order to avoid difficulties with solder holefill and thermal board damage encountered with Pb-free wave soldering of thick, complex printed circuit boards. Pending identification of instrumented connector insertion/extraction capability, the consortium will explore the reliability of compliant pin connections. Standard or microcompliant pin formats may be used depending on the preferences of participating Principals.

The project will include characterization of pin insertion and retention forces and subsequent examination of PCB structures in the vicinity of the PTH for internal damage. Possible assembly variables include pin finish (SnPb or Pb-free), plated through hole surface finish and finished hole diameter. The stability of retention forces will be monitored following board stresses of primary interest to the membership. These stressors may include hot gas rework of adjacent components or vibration loading of the assembly.

REL14A. Board Level Interconnect for 3D Stacked Die Package

As the shrinking of semiconductor technology nodes becomes ever more expensive, higher levels of system integration are now migrating to the package level. This increased package level integration takes the form of either multiple die with various functions on a common interposer (2.5D packaging) or a stacking of thinned die containing through silicon vias (3D packaging). The earliest industrial adopter of stacked die packaging technology has been the memory industry. While memory suppliers extensively test the reliability of the various first level interconnects in such 3D package structures, characterization of the reliability impact on the second (board) level interconnect is largely left to the customer.

Increased in-plane package stiffness associated with such large silicon die stacks is anticipated to degrade the thermal cycle reliability of the BGA interconnects relative to conventional single die BGA packages. This project will test the thermal cycle reliability of a representative stacked die BGA package using a stacked die memory package specially designed with an electrical continuity net stitched through the board level interconnects. A new test board must be designed and sourced to accommodate the device stitch nets. These boards will be assembled using common Pb-free SMT practices. Characteristic fatigue life under thermal cycle will be monitored along with the associated fatigue damage mechanisms as observed in the solder joint microstructure.

REL15A. Power Cycle Reliability

In recent years, the rationale behind thermal cycling reliability tests has been challenged because uniform heating and cooling of an electronic assembly is not representative of field use conditions. Rather, the heat dissipated in a powered device produces a temperature gradient within the

component, producing a different mechanical stress state. Further, the cycle time is much shorter which may affect the mechanical response of the interconnect. In 2015 the AREA Consortium will develop a test methodology for power cycling electronic components. Equipment for powering, monitoring, and controlling the experiment will be provided by a supporting consortium member. The test methodology will be designed to test the components until electrical failure after which failure analysis will be performed.

Assembly Process Development

It is no coincidence that a research organization with Universal Instruments has a focus on assembly process. By virtue of its access to surface mount manufacturing equipment, the AREA consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. As each of these areas become more sophisticated, AREA Principals have a continuous need to increase their understanding of the process windows for manufacturing and of design improvements that can be implemented to improve yields. To successfully introduce a new technology at high yields and low fallout, extensive research in process development is required.

On a separate but important note, for every component that is investigated, characterized, assembled, and tested, its information is uploaded to the AREA Component Database for easy and quick access in addition to the final project reports (http://www.uic-apl.com/databases).

APD1A. Broad Band Printing

As certain commodity components such as chip passives or memory devices migrate to finer and finer interconnect feature sizes, their use on large complex circuit boards poses ever increasing SMT process challenges. A large diversity of feature sizes placed within small distances on the board is beyond the capability of current solder paste printing methods. This project will quantify some of the limitations of paste printing methods to accommodate the wide ranges of feature sizes required when low and high density I/O SMT components are placed very near each other.

A test board will be designed for evaluating printing quality of fine components immediately adjacent to (or possibly within the footprint of) a coarse feature component such as a 1.27 mm pitch BGA. Fine feature components will include small passives devices and fine pitch CSPs with area array footprints. The board design will include continuity test nets for later use.

The subsequent project phase will consist of paste printing trials only. Automated paste inspection tools will be used to establish the limits of a quality print process across the full range of feature sizes and proximities included in the design. Printing process windows may be defined for different stencil thicknesses and paste types with other print parameters being held constant.

Board assembly trials can then be run using print parameters at the outer limits of the previously defined process windows. Assembly yields will be measured for marginal print conditions.

APD3A. Advanced Packaging Considerations

Design considerations for packages are being driven by electrical needs and space requirements. As a result, PoP and leadless device technology provide packaging companies with a means to optimize electrical performance while minimizing the space required. In the next generation of these components, not only are pad designs, materials sets and RDLs changing, but internal die sizes and distributions can no longer be assumed as symmetrical. This project consists of the ongoing acquisition of emerging component technologies and designing them into our test boards for process development and evaluation. Baseline board level reliability data do not exist for many of these types of packages nor does an understanding of PCB design considerations for high yield production and reliability. Three package types will be evaluated in 2015. A large 55mm x 55mm, 4300+ I/O BGA, a functional 132 lead Dual Row QFN with a large thermal pad, and a 56 lead multipad QFN device. Assemblies will be thermally cycled from -40/125°C with in-situ event detection. Samples will be removed from the chamber as they fail for failure analysis.

APD4B. Rework of MLF Devices

Low standoff Micro-LeadFrame packages (*a.k.a.* QFNs) are becoming more prevalent in our Principals' product designs. Discussions on this topic with many of our Principals indicate that no standard process exists. Suitable and reliable rework processes for such components require additional development. Moreover, second level solder joint reliability of replaced MLF devices is not well known.

The rework process for fine pitch and dual row MLF devices will be developed and its impact on reliability will be assessed. Of specific interest will be the contribution of solder joint voiding level (if any) on the thermal cycle performance. The TB2013 vehicle will be used.

APD6A. AOI/SPI Defect Detection

New advancements in AOI and SPI software and measurement techniques can be utilized for co-planarity measurements and volumetric calculations. As electronic devices become more complex they become susceptible to defects that are not necessarily detectable by standard inspection techniques. 3D x-ray systems can identify defects but they are slow and expensive to operate. In-line systems like SPI and AOI that have the ability to share data and make more complex evaluations of joint quality and component collapse may be a reliable alternative for defect detection. They can additionally be used to identify a process in danger of breakdown. AOI and SPI data collected from various other AREA projects will be analyzed for possible product defects and opportunities for process optimization. Other opportunities such as AOI co-planarity measurements will also be investigated as a method for identifying potential defects and reliability consequences.

APD9A. Warpage Contribution to Head on Pillow Defects

Higher solder melting temperatures and reduced wetting capability of Pb-free solders have dramatically increased the occurrence of Head on Pillow (HoP) BGA soldering defects in Pb-free assembly operations. This defect is characterized by a BGA solder ball lifting out of its intended solder paste deposit due to temperature induced distortion of the package (or circuit board) prior to solder melting. The BGA ball drops back into the solder on the board during cool down but does not wet to that solder deposit to form a coherent joint. For a fixed set of solder materials and reflow profile, the incidence of HoP defects is therefore expected to depend on the magnitude of temperature induced (or 'dynamic') warpage. The dynamic warpage characteristics of BGA packages are often such that a solder ball grid array which is nearly flat at room temperature will be distorted considerably out of plane at solder solidification temperatures.

A primary task of this project consists of designing and building laminate flip-chip BGA packages with controlled and reproducible dynamic warpage. This is to be achieved by varying the silicon die dimensions (including thickness), underfill materials, solder ball size, or other package attributes. The various BGA configurations thus generated will be subjected to shadow Moiré analysis to identify package warpage characteristics as a function of temperature. These BGA packages with different controlled warpage characteristics will then be assembled to rigid circuit boards using a common SAC305 solder paste and typical solder print deposit volumes. The assembled population will then be carefully inspected for Head on Pillow defects using industrial 3D xray inspection tools. Additional iterations of package design may be required to generate an adequate HoP 'signal'. Further process options, such as solder paste formulation, reflow profile and atmosphere may be required to reproducibly generate this defect.

Detecting Head on Pillow defects non-destructively is not trivial. The aid of consortium Principals has been enlisted to provide 5Dx and TRI inspections of the BGA solder joints. Statistical analysis of the HoP defect counts thus found will be used to determine the correlation between temperature induced warpage of the package and solder joint HoP defect rate. If those data indicate a threshold dynamic warpage for the onset of significant HoP defects, an additional project phase will be considered in which larger lots of controlled warpage components are assembled to evaluate HoP defect rates with improved statistical significance. Such data may be shared with the packaging industry at large if deemed beneficial to the membership.

Consortium Deliverables

The charter of the AREA Consortium is to convey the body of research performed and knowledge acquired directly to the Principals in a practically useful manner. This is achieved by providing information in various formats and transfer means including accessible databases, reports, recommendations, as well as design guidelines and test protocols.

Reporting of Results

The AREA manager and staff will provide access to project reports and experimental data via the protected consortium web site. Regular consortium meetings will be held in the greater Binghamton, NY area for the purpose of scientific/technical discussion. The AREA Manager and staff will inform Principals on specific technical issues, experimental results, or general project status. Presentations made at these meetings, with audio commentary, will be accessible on-line to Principal companies shortly thereafter. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. Project needs may require the AREA staff to solicit the involvement of suppliers as limited project participants but limit their access to knowledge generated on their products.