Advanced Process Laboratory, November 2013
ADVANCED RESEACH IN ELECTRONICS ASSEMBLY
Consortium 2014 Research Plan

EXECUTIVE SUMMARY

The Advanced Research in Electronics Assembly (AREA) Consortium will fund manufacturing relevant research to provide AREA Principals' an understanding of emerging technologies in materials, reliability and assembly process. The breadth of the research plan spans academic focused research to topics that directly apply to current manufacturing needs. It is our objective to provide AREA Principals with data that enables sustainable process improvements in conjunction with maximizing yields and optimizing product reliability.

The AREA Consortium staff understands that in the current business climate our Principals have little time to devote to research beyond critical product needs. Therefore Principals of the AREA Consortium view the consortium staff as an extension of their own engineering team devoting critical research time and physical resources to emerging topics of interest. To support the efforts of providing Principals with the most up-to-date information, project milestones and instant access, a comprehensive website with on-demand content is available. (http://www.uic-apl.com/).

The AREA consortium research plan is principal driven, consortium manager prioritized, and consortium staff executed. The focus of research is based on current and near future needs of the electronics manufacturing industry. This research plan is updated annually so that topics remain relevant and pragmatic. The AREA manager and staff develop the research plan in close partnership with AREA Principals and AREA Steering Committee (http://www.uic-apl.com/home/area-steering-committee). The AREA manager and staff execute the plan utilizing the resources of UIC's Advanced Process Lab.

The primary focus for 2014 will be the initiation and/or the completion of the projects outlined in this document. Additional topics are added throughout the year as materials are provided and interests develop given that resources are available. The 2014 research plan for topics in Materials, Reliability, and Assembly Process will be described throughout this document.

Contents

Project Goal

The goal for a specific project is to provide knowledge, understanding and tools for the design of products, selection of materials, development of manufacturing processes and testing to ensure an optimum combination of quality, reliability, low cost and high yields. The work is conducted in a systematic, logical and scientific manner with supporting documentation of adequate test data to allow reproducible results in an R&D or manufacturing environment. In any given project, the AREA consortium investigator looks to systematic identify, characterize and provide information on the behavior of a process or material. This knowledge assists the AREA Principal in realizing an effective transfer of a particular process or technique to other related products.

Consortium Structure & Function

The AREA Consortium is organized and managed by Universal Instruments Corporation, Conklin, NY.

Two types of companies, Principals and Participants, support the AREA Consortium. A Principal is a corporation that provides financial support to the Consortium funded work and receives a complete copy of the progress reports and final documentation. A Participant is a corporation that does not contribute financial support, but provides material and/or product development to the Consortium. A Participant receives limited information related only to the contributed materials. No proprietary information pertaining to competitive Participants involved in the study is communicated verbally or in writing to other Participants in the study. Wherever possible the AREA manager and staff will utilize properly supported data generated by Principals, Participants or other reputable sources.

Plans

The research that the AREA Consortium conducts is broken down into three major concentrations. These areas span topics of academic interest and scope as well as topics that are directly applicable to current or near future industrial needs in materials evaluations, reliability testing and procedures and assembly process development.

The intent of this document is to define the scope of a given project, Figure 1. All these topics are based upon either existing projects continuing in 2014 or project proposals that are under development. The 2014 Research Plan is complemented by separate and more project focused Proposals which include a definition of objectives, test design and deliverables for many of the projects derived from this research plan, Figure 2. The Proposals related to a specific project are available by contacting the AREA Consortium staff or accessing our comprehensive website (http://www.uic-apl.com/).

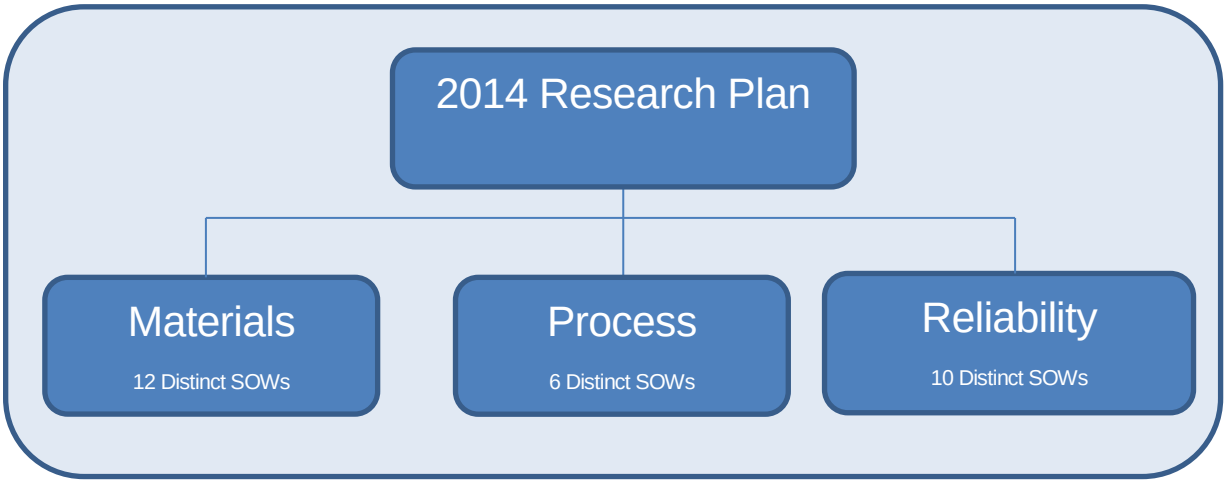

Figure 1. The 2014 AREA Research Plan

Figure 2. The 2014 Research Proposal Structure

Projects are defined by a Scope of Work (SOW) and sequentially grouped into the appropriate research focus. In addition, all material and assembly process related research is subjected to and evaluated by mechanical and/or thermal accelerated life testing. Therefore many of the following material and assembly process descriptions include relevant reliability testing in order to achieve the objectives of that research. Reliability research is segregated into topics specifically related to test procedures and protocols for the purpose of producing meaningful data for a given reliability test.

Materials

Innovations in materials make the job for designers and assemblers both easier and more complex simultaneously. Advances in material science provide manufacturers with tools to optimize process and increase yield. However, the breadth of material types and the demand for miniaturization, results in a significant challenge for adopting these emerging technologies. AREA Principals are faced with evaluating the properties of these materials, the assembly process window and performance in accelerated tests. The focus of the AREA Consortium is to provide the Principals relevant and timely information on selected materials to address these needs. The AREA Consortium utilizes a systematic, scientific approach to perform evaluations that are both comprehensive and comparative in nature. A thorough characterization of the materials under investigation is assessed in an attempt to define the material process windows and impact on reliability.

MAT1A. Underfills and Adhesives

On this subject, the focus of the research in this field of study is a continuation of the systematic evaluation of various capillary underfills including reworkable materials. An important subject of study for each capillary underfill will be its compatibility with flux residues and flow behavior. Materials for this investigation will be acquired from multiple suppliers. Components of various designs (BGAs and LGAs) are represented on the 2013 AREA Consortium test board for use in these studies. Consequently, the goal of this investigation is to provide directly applicable insight on flow characteristics and voiding under typical and low standoff components. These capillary underfills and reworkable materials will be subjected to reliability testing by accelerated thermal cycling. The investigation of underfill adhesion behavior on various solder mask materials available to the industry will be a longer-term goal and depends on the cooperation of the Principals.

Another aspect to this topic will be the investigation of conductive adhesives. The extent to which this subject will be covered depends on materials supplied by the Principals. However, we expect to perform material characterizations of several commonly used materials in the industry for adhesion and reliability in various mechanical and thermo-mechanical testing conditions.

MAT2A.Circuit Board Materials

The AREA Consortium continues to acquire new board laminates from various board vendors. As a result, each board laminate will be subjected to a quantitative characterization to evaluate their robustness utilizing mechanical and thermal test methods. The primary focus of this investigation is to identify the degree of pad cratering and thermally induced degradation.

A secondary effort in this field of study is to develop a standardized test procedure and the design of a standard test vehicle for all future board evaluations in an attempt to standardize the evaluation of materials. The resulting design and test method will be an extension of current methods. An important objective of this study is to provide AREA Principals a method that can be internally adopted for the submission and evaluation of future materials.

MAT2B: Pad Cratering Dependence on Glass Type

AREA research in 2013 ascertained that a pad's strength and fatigue life depends on multiple factors. Two of these are: its location relative to the glass bundle under it and the details of the glass weave itself. The tightness of the weave, i.e. the presence or absence of resin-only regions, was among the parameters studied. The effects of these laminate characteristics were demonstrated in studies comparing two different laminates. The goal for this field of study is to extend our understanding as well as to include various glass styles being adopted for the test vehicles of the planned HDI project

MAT3A. Surface Finishes

A large number of new surface finishes have been made available to the electronics industry in the recent past. The AREA Consortium provided process and reliability comparisons for several of the common set of materials such as ENEPIG, lead-free HASL, OSP (ENTEK OM), Pallaguard, and others, in 2013.

The objectives for work in this field of study are to complete these evaluations through thermal cycling reliability with a final report delivered. In addition, a considerable effort into microstructural analysis and its failure mechanisms for solder joints of various volumes and configurations will be undertaken. This data can be used by our Principals in evaluating the various failure modes associated with these surface finishes in lead-free soldering applications.

MAT4A. Thermal Interface Materials (TIMs)

As logic speeds continue to increase the need to remove heat from high end electronics is becoming more of a challenge with standard TIMs. In addition material degradation in field is a significant risk for the performance of electronics expected to remain in field in excess of 20 years. This research intends to evaluate current gap pad materials and suppliers for evidence of degradation under thermal storage and ATC testing.

The objective of this research is to continue the systematic thermal interface material evaluations utilizing our 2012 component level test vehicle. The goal of this project is to provide a comparison between the various gap pad materials and suppliers while controlling pressures and separations in thermal cycling.

MAT5A. Paste and Flux Evaluations

A standard protocol for paste and flux characterization will be established in 2014 using typical industry standards as well as a particular PCB design representing current component technology. The goal of work in this field of study is characterize the impact of component pitch and pad design on print transfer efficiency. A standardized test board will be utilized to study these material sets.

High Temperature Electronics Research Overview

As electronics become integrated into higher temperature environments such as those associated with deep well drilling, and distributed controls in the automotive and aviation applications, higher melting temperature alternatives are needed. This program, outlined at the September 2013 AREA Consortium Meeting, will focus on the materials, assembly, and reliability of high temperature electronics packaging. To support this work, a high temperature polyimide test board was designed with specific features (http://www.uic-apl.com/board-designs).

MAT6B. Die Attach and New LF Alloys

High temperature die attach materials are mission critical for the operation of next generation power semiconductor devices. These products operate at substantially higher temperatures than conventional electronics. With the expiring Restriction of Hazardous Substances (RoHS) exemptions, it is now imperative to consider Pb-free alternatives even for high temperature applications. The focus of work in this field of study will be a continuation of joint level strength, reliability, and microstructure evaluations. Various types of die attach materials will be studied and characterized for their viability as drop-in replacements or perform "as good as" current materials. The materials included in this investigation consist of alloy pastes, sintered pastes, metal filled epoxies, and new Pb-free alloys developed in conjunction with Binghamton University.

MAT6C. Second Level Process Development and Material Evaluation

Utilizing the high temperature test board designed in 2013, various high temperature alloys will be compared in terms of alloy microstructure and resulting reliability in ATC test. Current industry practice is to hand solder many of these devices resulting in a high level of variability in its solder volume and consequently thermal history. The focus of research in this area of study is to utilize solder paste and high temperature convection soldering to systematically control the temperature and paste volume. The objective is to have the ability to compare and interpret results from accelerated testing for the materials evaluated. This will further our understanding and allow for more controlled assembly recommendations.

MAT7A. New Lead-Free Solder Alloy Evaluations & Microstructure

Lead Free alloys with various concentrations of dopants are currently being evaluated by the industry as drop-in replacements to the standard SAC305. Suppliers claim that dopants in these alloys results in improved drop test performance. In addition, these doped materials are less expensive due to lower silver content. Our previous results have shown that mechanical and thermal reliability improvements can be correlated to microstructural differences created by varying solder volume and PCB surface finish. Significant effect of solder volume and composition on microstructure and thermomechanical performance of various lead free solder joints was observed.

The focus in this field of study will be a continuation in the evaluation of microstructure and mechanical properties for various solder alloys on different pad finishes. This aspect will encompass performing characterizations for both individual solder balls as well as components assembled onto test boards for true second level reliability comparisons, either by ATC or mechanical testing. It is also planned to evaluate other alloys that were only available in the form of paste such as Innolot (90iSC) and SAC0307 alloys.

Another objective of this work is to quantify the performance of new lead free solder joints as compared to SAC 305 and SnPb alloys. Included in this work are the addition of a SnPb control and a mixed technology build consisting of lead-free solder joints and SnPb paste.

MAT7B. Effect of Reflow Profile on Mechanical Properties of Various Solder Alloys

Our recent results have shown that room temperature fatigue tests display promise as a relatively simple and sensitive means to monitor the effect of different parameters on solder joint reliability. It is possible to see the effect of solder composition on shear fatigue performance and correlate it to results obtained from ATC tests. The focus of research in this area of study is threefold. First, a controlled investigation studying the effect of solder joint composition and thermal history, including peak reflow temperature, time above liquidus and cooling rate, on fatigue life time of solder joints will be examined. Second, characterization of these solder joints will be conducted at room temperature as well as at high temperatures. Third, a modeling effort is planned to further investigate the testing parameters such as strain rate on fatigue behavior. The objectives of this investigation are to potentially elucidate the reason for early failure of joints in test. Additionally, this investigation may provide guidance on how process parameters are optimized to obtain more reliable solder joints.

MAT7C. Effect of Precipitate Size and Spacing on Thermal Fatigue Performance of LF Solder Joints

There is a clear need to have a microstructurally adaptive model to be able to predict life time of solder joints. It is well known that size and spacing of precipitates (Ag3Sn and Cu6Sn5) can affect the thermomechanical performance of solder joints. Joints with a larger number of smaller sized precipitates exhibit higher strength and increased resistance to

creep and fatigue. Our recent results have shown that indeed solidification temperature of lead free solder joints can affect the size and spacing of precipitates and thus the fatigue performance of joints. Isothermal pre-aging will significantly change the size of precipitates. The larger precipitates grow in expense of smaller precipitates. Growth of precipitated could affect the recrystallization behavior during thermal cycling test and expected to degrade the reliability of joints. However, current available data shows discrepancies on the effect of isothermal pre-aging. We are in the process of quantifying, in a strictly controlled manner, the size and spacing of precipitates as a function of solder composition and volume after reflow and also during isothermal aging at various times. The effect of strain enhanced coarsening during ATC test for joints will be quantified as well. The results could be used to develop a constitutive model to predict the life time of solder joints.

MAT8A. Conformal Coating

As more high reliability Telecommunications Enterprise OEMs deploy their products into remote areas of the world, they can no longer ensure that proper environmental controls are established for their high end products. As a result, these technologies that have already adopted lead free materials are now forced to consider conformal coating as an added protection against corrosive environments. Our efforts in conformal coating research intended to help our Principals understand the effect of coatings on the accelerated testing typically used for qualification of products. Principals have highlighted interest in other classes of materials such as parylene which will be considered assuming cooperation of our Principals.

This topic also has value for our military Principals in the context of component miniaturization. As military products are forced to adopt finer pitch devices and low standoff components for speed and obsolescence reasons, the impact of conformal coating on ESS testing has become a challenge. Conformal coat stresses on second level interconnects are causing early life failures resulting in expensive rework and pre-deployment process changes that have not been properly characterized and vetted. The focus of work in this field of study is to continue our research specifically into SnPb solder assemblies.

Reliability

The AREA Consortium efforts into reliability are more fundamental than simply testing materials under certain reliability test procedures and conditions. Our Principals are often forced into situations where accelerated life testing is a requirement. The majority of descriptions for these methods are incomplete. In addition, little data exists for the assembly and design aspects of the test that results in the greatest effect on the reliability. The AREA Consortium has developed a fundamental understanding of reliability, test methods and material behaviors under various stress conditions. The projects described in this section are, as a result of our Principals requests, to better understand both the test methodology and the failure modes generated while quantifying their impact on reliability.

REL1A. Prestress & Pad Cratering

Over the course of the past year, the AREA consortium undertook an investigation to study the acceleration factors of cyclic bend, drop and vibration following PCB pre-stress using the spherical bend test methodology (IPC/JEDEC-9707). As part of the discovery in this nontrivial work, various issues were uncovered with both the test method and test vehicle. The results were unexpected failure modes and limited acceleration of failure under various stress conditions. The focus of work in this field of study will be a continuation in the improvement of the test method to initiate pad cratering followed by accelerated testing.

REL2A. Lead-Free Phenomenological Model

The interpretation of 'engineering tests' as well as the quantitative prediction of life in service require a mechanistic understanding and practical models. So far, our research has shown current thermal cycling models and acceleration factors to break down and be potentially misleading when it comes to lead free solder joints. A general mechanistic understanding has been established. We have also shown the rate controlling mechanisms to be very different for solder fatigue failure in isothermal cycling. A phenomenological approach to the extrapolation of accelerated test results to life in cycling with different, but still constant, amplitude has been proposed and validated. However, realistic service conditions rarely

involve constant cycling amplitude. We have shown Miner's rule and other current damage accumulation rules to break down, in some cases overestimating life by an order of magnitude or more.

Based on a systematic mechanistic study, a first phenomenological model is emerging which allow the prediction of life for combinations of isothermal cycling amplitudes. Work is ongoing to extend this to include interpolations and extrapolations to other amplitudes. Further studies will address effects of strain rates, alloys and aging.

The low cycle fatigue life of SnAgCu solder joints may be reasonably well approximated as the number of cycles required to do a certain amount on work on the solder. However, this does not allow for the direct calculation of life or the extrapolation of accelerated test results to lower cycling amplitudes, because the constitutive relations vary with amplitude. The consequences remain limited, albeit significant, for cycling with a fixed amplitude. The situation is much worse for cycling with varying amplitudes, where the overall life may end up orders of magnitude lower than predicted based on Miner's rule. In fact, all currently available damage accumulation rules break down when it comes to this. We are in the process of documenting why the only realistic solution is to base a new rule on a mechanistic understanding. Systematic EBSD and TEM studies to, among other, correlate the interaction effects with Sn grain orientations, are expected to significantly improve on our fundamental understanding. In the long term this will be critical for confidence in extrapolations to service conditions.

Meanwhile, a semi-empirical rule has been shown to be successful in predicting life in accelerated testing when the cycling amplitude is varied repeatedly between any two values. Different solder alloys have shown different sensitivity to variations. Work on SnPb and effects of aging will also be evaluated. Work is ongoing to extend the rule to any combination of three different values. The rules will be applied to illustrate effects of variations during random vibration, including differences between typical and worst case combinations.

Further efforts will focus on how to extrapolate results to the lower amplitudes typical of long term service conditions. Results will demonstrate how accelerated vibration experiments may be extremely misleading when it comes to predictions of life under realistic conditions, and how the best predictions would be based on results of fixed amplitude cycling and simple combinations of amplitudes. It will be shown how to properly conduct and interpret accelerated test results.

REL3A. Vibration and Drop Testing Methodologies

Vibration testing has been employed by the high-cycle reliability segment of the electronics industry with concerns regarding product performance due to vibration-related manufacturing, transportation, and end-use conditions. Standards are available for vibration testing such as JESD22-B103B and MIL-STD-810G Method 514.6 – Vibration. Generally, these provide vibration testing guidelines for material development, reliability metrics, and qualification purposes. These standards do not provide methods for building solder fatigue data and consequently are limited to very specific products and testing conditions. A comprehensive testing and modeling approach is needed develop high-fidelity fatigue data (i.e., S-N curves) that can subsequently be used to explore a much wider range of test conditions and product configurations.

From our failure analysis efforts in 2013, we identified some critical limitations to the detection of failures using current event detection methods. The focus of work in this field of study will be to evaluate detection strategies while duplicating some of the resonance tracking efforts completed in 2013. The objective of this work is to qualify and prove fidelity of these new techniques in detecting failures as they occur in vibration testing.

REL4A. Creep Corrosion

Flowers of Sulfur (FoS) testing is seeing increased use as a simpler, easier and more economical alternative to Mixed Flowing Gas (MFG) for studying creep corrosion. However, it is considered less representative of a realistic corrosive environment. As a result, it is not, at present, considered a viable qualification tool. Yet, it is more useful as a technique for screening various materials, including pad finishes, solder masks, and fluxes or pastes with potentially corrosive residues. However considerable discussion is being generated within the industry about improving it as a test method by introducing stirring or internal air circulation at different flow rates. Also under consideration are ways of intentionally exposing samples to certain "model" contaminants such as sodium chloride at various concentrations or compounds found in industrial dust. The focus of research in this field of work is twofold. The first objective is to investigate the impact such experimental variables exert on the corrosion response, creep or otherwise. The second objective is the continuation of testing utilizing the existing technique to characterize those materials of interest to Principals.

REL6A. Print Correlations to Reliability

The Advanced Process Laboratory is equipped with state-of-the-art solder paste inspection (SPI) technology. Utilizing this capability, all AREA consortium PCB assembly based projects that include stencil-printed boards will be characterized by this tool. A comprehensive collection of paste volume, area, and height data has been collected in 2013. As reliability data is collected, failure trends will be analyzed and correlated to the information acquired with stencil printing volume measurements. The goal of this research is to provide an understanding of stencil print process window sensitivity for various classes of devices based on the statistical analysis of SPI results.

REL9A. PCB HDI Robustness

As electronic devices continue to shrink, circuit board routing designs require evaluations to better understand their effects on component reliability. The focus of work in this field of study is to investigate micro via designs that include various via stacking arrangements. Once these boards are assembled, the PCB's will be subjected to various accelerated tests including thermal shock and mechanical testing. The objective of this research is to evaluate the robustness of the micro via stacking. This investigation will focus on characteristic board designs from the hand-held devices and military industry segments.

REL10A. Drop test JESD22-B111 Redesign Evaluation

Drop testing standard JESD22-B111 is expected to change in early 2014. The impact of this change is significant. This affects the complete supply chain – from supplier to OEM. First, an understanding of the changes is required, followed by characterizing materials utilizing the new protocol. The focus and goal of work in this field of study is to perform A to B comparisons of these changes in order to assess the impact on joint performance for various component types.

REL11A. Compression of Second Level Interconnects and the Effect on ATC Reliability

The thermal performance of certain types of thermal interface materials (TIMs) is pressure sensitive. Previous consortium research has shown the thermal resistance for

gap pad materials decreases with increased pressure (http://www.uic-apl.com/meetings/2013-meetings). The rule of thumb is 30% TIM compression is a good tradeoff between increased thermal performance and acceptable component reliability. However the relationship between TIM compression pressure applied to a BGA is not fully understood and warrants further study.

A new test vehicle is being designed to evaluate the effect of compression of second level interconnects. Devices in high speed products that require thermal dissipation in the form of heat sinks are often placed under considerable compressive loads. This test vehicle will systematically vary the compressive loads to evaluate these effects. This test vehicle provides us insight into the effect compressive loads on the second level reliability of surface mount components.

Assembly Process Development

It is no coincidence that a research organization with Universal Instruments has a focus on assembly process. By virtue of its access to surface mount manufacturing equipment, the AREA consortium is uniquely suited to develop manufacturing processes for emerging technologies in component, materials, and board designs. As each of these areas become more sophisticated, AREA Principals have a continuous need to increase their understanding of the process windows for manufacturing and of design improvements that can be implemented to improve yields. To successfully introduce a new technology at high yields and low fallout, extensive research in process development is required.

On a separate but important note, for every component that is investigated, characterized, assembled, and tested, its information is uploaded to the AREA Component Database for easy and quick access in addition to the final project reports (http://www.uic-apl.com/databases).

APD1A. Broad Band Printing

Continued adoption of finer pitch components (i.e. 0.25mm pitch, 01005, etc.) stretches the gap between low and high density I/O components. In 2013, a 0.3mm test board was designed to pursue stencil printing process improvement strategies. New stencil technologies, printing advances, and design considerations to provide best practices for manufacturing were identified to extend the typical print aspect ratios. The focus of work in this field of study will attempt to develop a list of criteria for each of our Principal markets that describe broad band processing. This definition will assist with future broad band research topics for specific markets.

APD3A.Advanced Packaging Considerations

Design considerations for packages are being driven by electrical needs and space requirements. As a result, PoP and leadless device technology provide packaging companies with a solution to maximizing electrical performance and minimizing the space requirements. In the next generation of these components, not only are pad designs, materials sets and RDLs changing, but internal die sizes and distributions can no longer be assumed as symmetrical. Baseline reliability data does not exist for these types of packages nor does an understanding of the PCB design considerations for high yield

production and reliability. The focus of work in this field of study will be a continuation in acquiring emerging component technologies and designing them into our test boards for process development and evaluation.

APD4B. Rework of MLF Devices

Fine pitch, low standoff devices are continuing to become more prevalent in our Principal's designs. As they are incorporated the need for a suitable and reliable rework process requires development. Discussions on this topic with many of our Principals indicate that no standard process exists. In addition, second level solder joint reliability of replaced devices is essentially unknown.

The rework process for fine pitch and dual row MLF devices will be developed and its impact on reliability will be assessed. The fine pitch devices previously assembled to TB2013 will be utilized in this investigation since significant thermal reliability data has been collected.

APD6A.AOI/SPI Defect Detection

New advancements in AOI and SPI software and measurement techniques can be utilized for coplanarity measurements and volumetric calculations. As electronic devices become more complex they become susceptible to defects that are not necessarily detectable by standard inspection techniques. 3D x-ray systems can identify defects. However, they are slow and expensive to operate. In-line systems like SPI and AOI that have the ability to share data and make more complex evaluations of joint quality and component collapse may be a reliable alternative for defect detection. Alternatively they can be used to identify a process in danger of breakdown. The focus of work in this field of study includes evaluating placement and print variations in 0201 assembly that can be detected by SPI and AOI as a guideline for process development. Other opportunities such as AOI coplanarity measurements will also be investigated as a method for detecting defects and affecting reliability.

APD7A. Hand Solder Process for High Temperature Electronics

Many components used in high temperature electronics can't withstand the temperatures of a conventional convection reflow process. For this reason HMP solder joints are typically

reflowed by hand using a soldering iron and board preheater. Contract Manufacturers have reported difficulty with reproducibility, joint cracking, and various other solder joint defects when a hand soldering process is used. The goal of this investigation is to develop a repeatable hand soldering process for various surface mount and through-hole components. The process will be systematically developed by varying tip parameters, as well as preheat and cool down profiles.

Finite Element Modeling (FEM)

The focus, for the AREA Consortium in FEM, is to continue assessing AREA test vehicles in modeling. Modeling is often used to identify high risk locations on products for possible failure locations; however model accuracy is always questioned. Much of the AREA Consortium efforts with a modeling focus are based on collaboration with Binghamton University to develop accurate models of our test vehicles. The goals are to develop S-N relationships for mechanical tests and aim to further our sophistication of the model to better predict mechanical stress conditions in vibration and drop testing. Ultimately these methods can be used by our Principals to provide greater insight into their products in support of design engineers developing emerging products and technologies.

Support of REL3A. Vibration and Drop Testing Methodologies

Advances in modeling techniques have led to high-fidelity models that faithfully replicate the dynamic characteristics of the test assemblies. Combined with novel modeling techniques, accurate stress analysis of critical failure locations can be obtained to support harmonic vibration testing (development of S-N curves). The goal of this investigation is to utilize the test boards, previously assembled for our vibration tests, for modeling efforts in order to estimate the stresses exerted on solder joints.

Support of REL11A. Compression of Second Level Interconnects and the Effect on ATC Reliability

The test board for evaluating the solder joint compression impact on thermal cycling reliability will be modeled for correlation to experimental data. The objective is to compare the effects of various compression designs and failure locations in thermal cycling. Development of finite element models simulates the effects of mechanical load and thermo-mechanical stress. Standard solder failure metrics, such as cyclic plastic work, will be used to compare designs.

Support of MAT7B. Effect of Reflow Profile on Mechanical Properties of Various Solder Alloys

As mentioned previously in MAT7B, a modeling effort to evaluate specific testing parameters exerted in any given shear fatigue test will be undertaken. This modeling effort identifies the stress conditions exerted on the solder joint as a function of the component stress condition. The objective of this ambitious modeling project is to simulate the cyclic shear test to determine deformation and stress patterns. The goal is to potentially provide insight into the failure mechanisms observed for this style of testing. This research will contribute to the ultimate objective of MAT7B to potentially elucidate the reason for early failure of joints in test and optimize process parameters for improved solder joint reliability.

Deliverables

The intrinsic value of AREA research is to convey the body of research performed and knowledge acquired directly and practically useful to the Principals in their daily work. This is achieved by providing various forms of information organization and transfer such as databases, reports, recommendations, as well as design guidelines and test protocols.

Reports

The AREA manager and staff continue to provide access to the reports and data via a protected web site. This year three meetings will be held in the greater Binghamton, NY, area for the purposes of scientific/technical discussions. The AREA Manager and staff will inform Principals on specific technical issues or general project status. These will be held in February, June and October. Presentations made at these meetings, with audio commentary, will soon be accessible on-line to Principal companies. In addition, Principals are encouraged to contact and/or visit the Advanced Process Laboratory individually for more effective communication and knowledge transfer. As before, the complete AREA team will also solicit the involvement of suppliers as Participants but limit their access to knowledge generated on their products.

Commitment Time Line

The activity above shall commence on January 1, 2014 and will be complete on December 31, 2014. A Principal's company on a calendar year membership schedule is asked for a

commitment in the form of a purchase order by November 15, 2013 to prevent any budget shortfalls. The AREA consortium is, however, not requesting payment until the 2014 calendar year. Also, this payment can be made on a schedule corresponding with your budget cycle. The November 15, 2013, 'deadline' does not mean that you cannot join after that, but it does mean that the budget will be largely established by that date.

Conclusion

The AREA Consortium will continue to be a resource for our Principals. The entire AREA team is constantly furthering our knowledge on the challenges in electronics assembly to better equip and assist our Principals. To this end, we expect to work in conjunction with AREA Principals in developing the next level of process understanding, development of designs and production of test data. The entire AREA team takes pride on being an extension of our Principals' engineering departments. We expect to continue to be a ***constant*** resource for our Principal in 2014.

Sincerely,
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